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Brand:	**Crumar**
Model	**DS-2**
Product:	**Digital Synthesizer**
Description:	**Schematic**

Musicparts Document Number: 47900 TechTips: No Pages: 36 Dated: None

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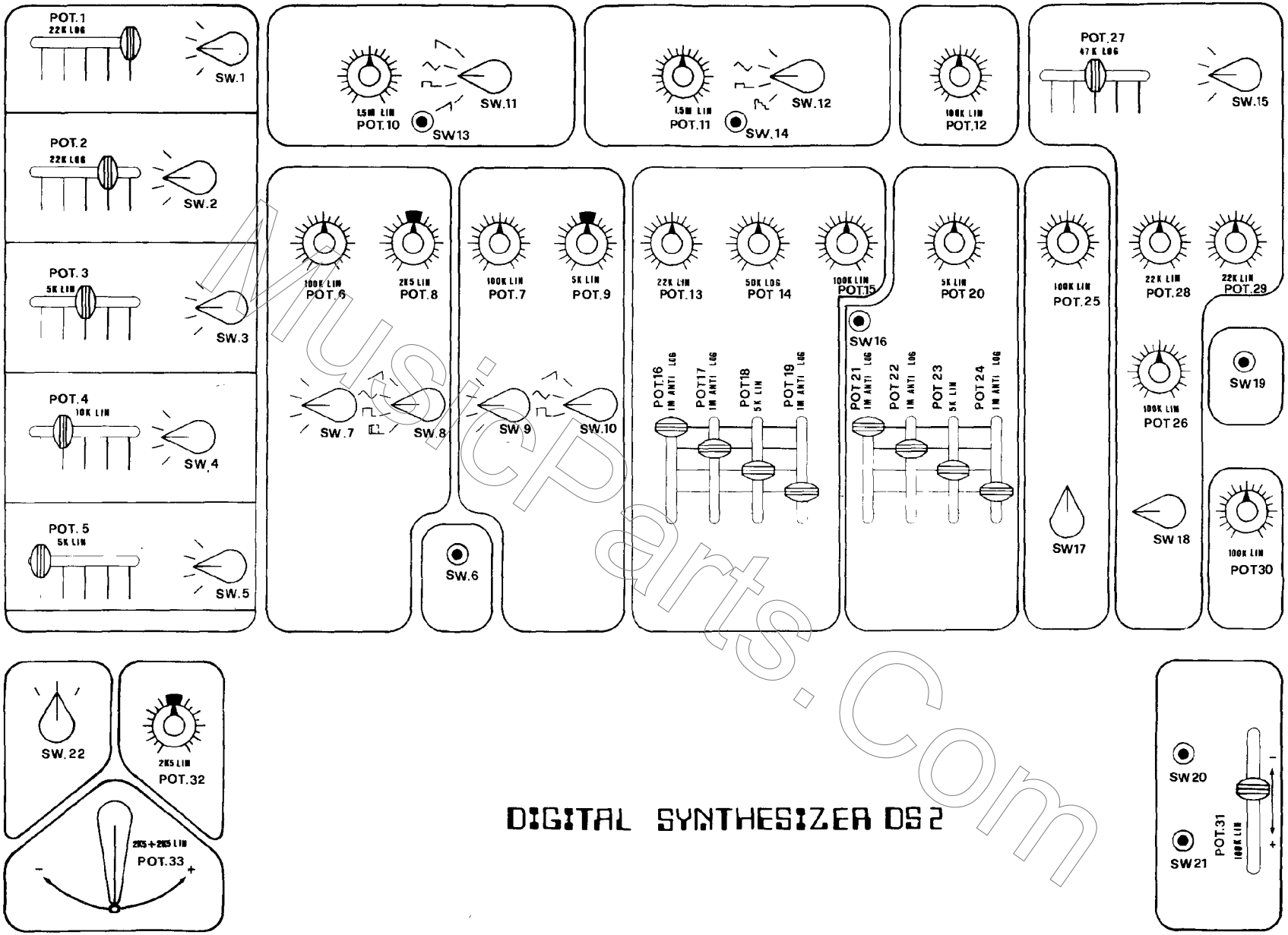
SCHEMATIC DIAGRAM

CRUMAR®

Musical Instruments

mod.

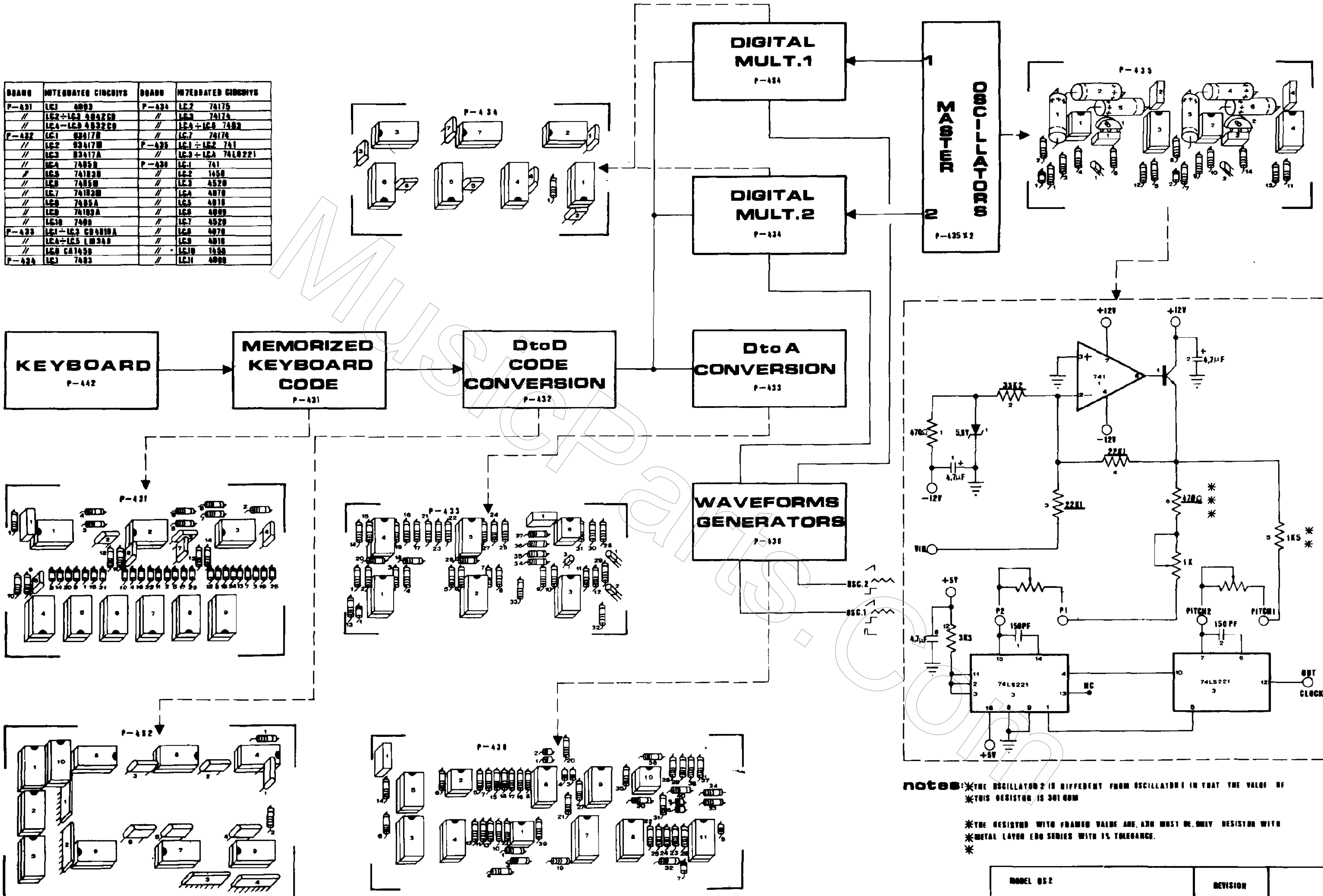
DS-2



DIGITAL SYNTHESIZER DS2

MODEL DS2			REVISION:
DATE 27-1-78	DRAWN BY G. Bordai	DESIGNED BY P. Kiraly	DATE

DWG 1



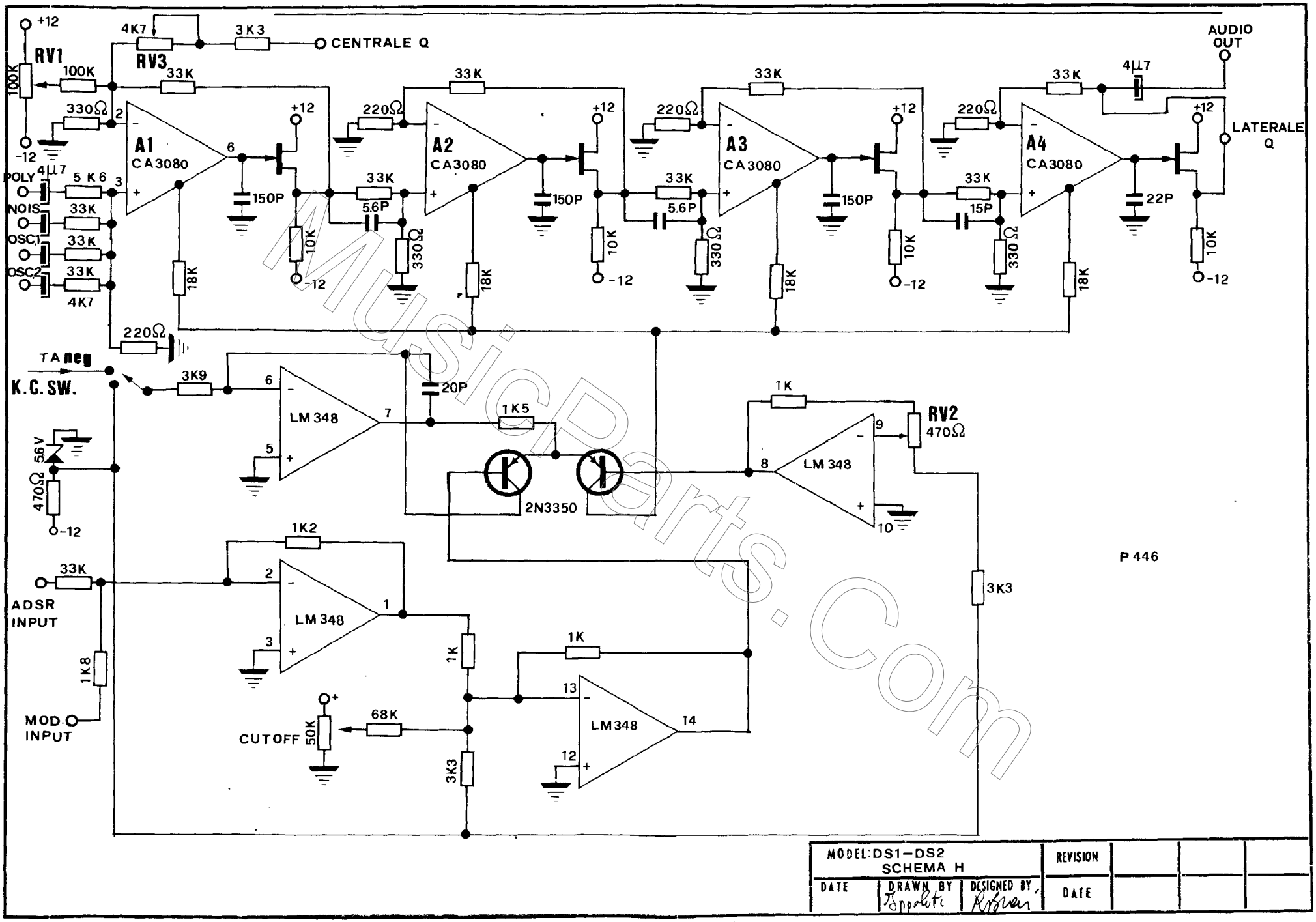
BOARD	INTEGRATED CIRCUITS	BOARD	INTEGRATED CIRCUITS
P-431	IC1 4093	P-434	IC2 74175
//	IC2÷IC3 4042CD	//	IC3 74174
//	IC4÷IC8 4532CD	//	IC4÷IC6 7483
P-432	IC1 93417B	//	IC7 74174
//	IC2 93417B	P-435	IC1÷IC2 741
//	IC3 93417A	//	IC3÷IC4 74LS221
//	IC4 7485N	P-436	IC1 741
//	IC5 74193N	//	IC2 1458
//	IC6 7485N	//	IC3 4520
//	IC7 74193N	//	IC4 4070
//	IC8 7485A	//	IC5 4016
//	IC9 74193A	//	IC6 4069
//	IC10 7400	//	IC7 4520
P-433	IC1÷IC3 CD4010A	//	IC8 4070
//	IC4÷IC5 LM340	//	IC9 4016
//	IC6 CA1458	//	IC10 1458
P-434	IC1 7483	//	IC11 4006

notes: ✱THE OSCILLATOR 2 IS DIFFERENT FROM OSCILLATOR 1 IN THAT THE VALUE OF
✱THIS RESISTOR IS 301 OHM

✱THE RESISTOR WITH FRAMED VALUE ARE, AND MUST BE, ONLY RESISTOR WITH
✱METAL LAYER E80 SERIES WITH 1% TOLERANCE.
✱

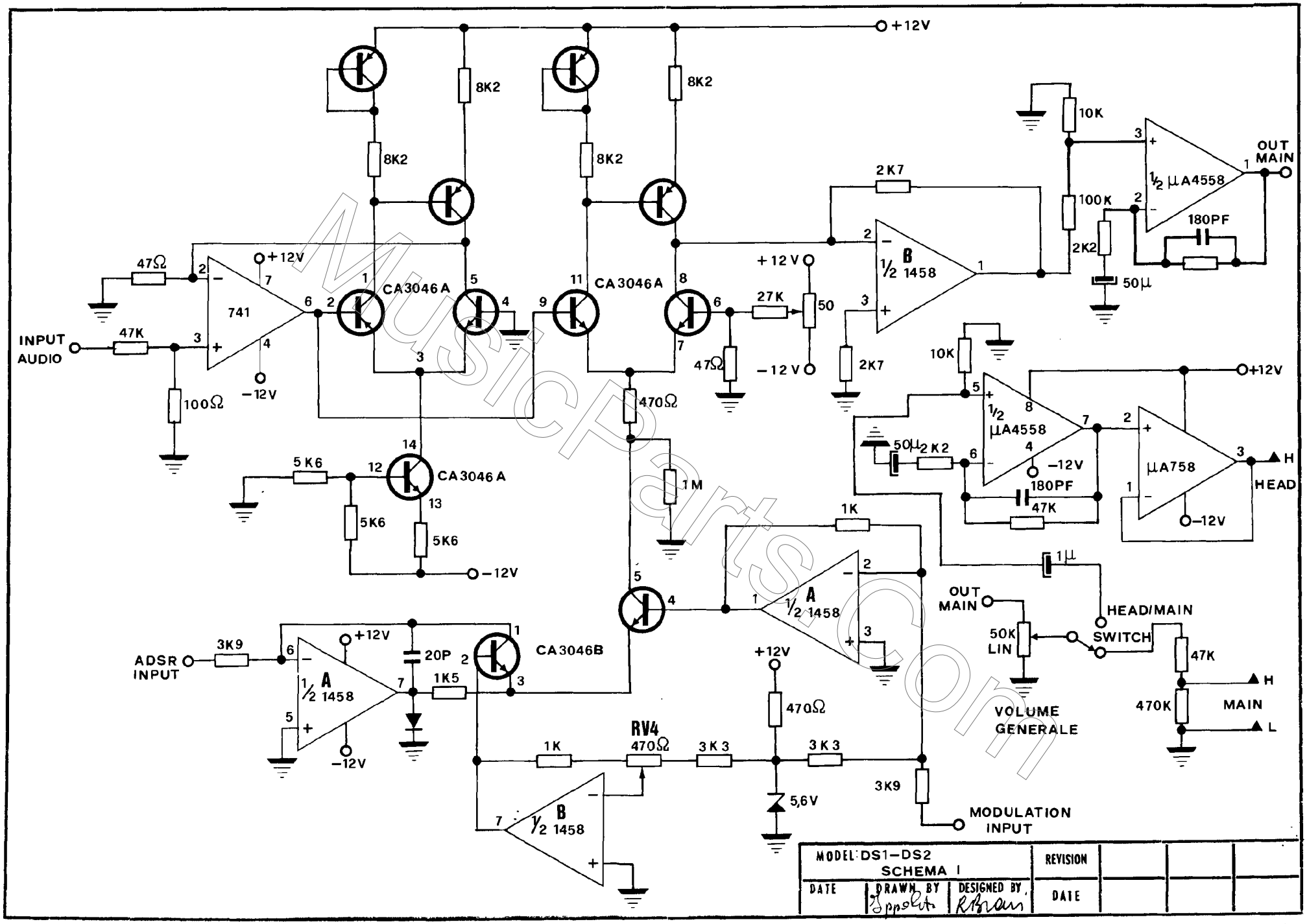
MODEL OS2			REVISION	
DATE. 27-1-10	DRAWN BY: S Bordini	DESIGNED BY R Braun	DATE	

DWG 2



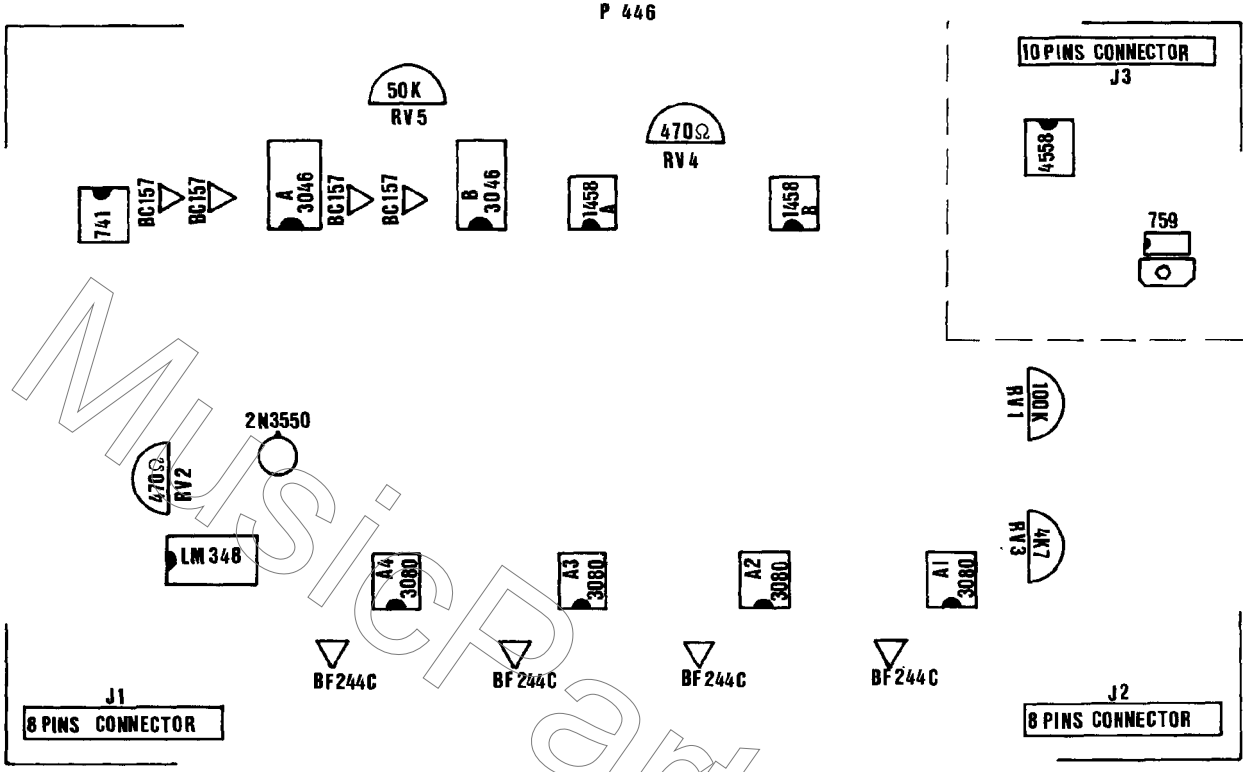
MODEL: DS1–DS2 SCHEMA H			REVISION			
DATE	DRAWN BY Spoletti	DESIGNED BY Rossi	DATE			

DWG3



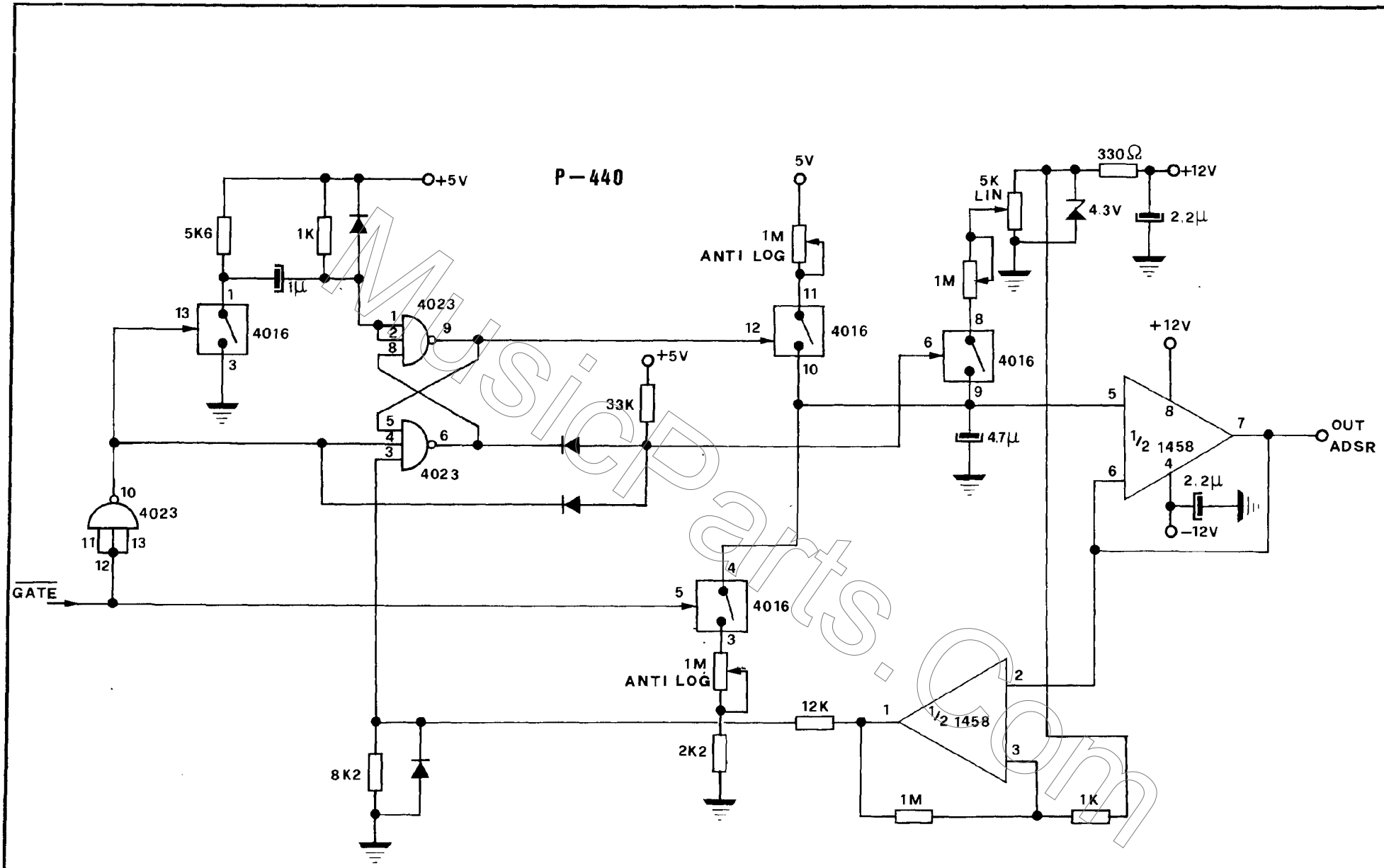
MODEL: DS1–DS2 SCHEMA 1			REVISION			
DATE	DRAWN BY Ippolito	DESIGNED BY R Brun	DATE			

DWG4



PIN	REFERENCE J1	PIN	REFERENCE J2	PIN	REFERENCE J3
1	−5,6V	1-2	GND	1	ADSR VCA
2	CUTOFF POT	3	RESON CENTR.	2	MODULAT INPUT
3	GND	4	POLY	3	−12V
4	MODULAT INPUT	5	NOISE	4	+12V
5	ADSR VCF	6	OSC 1	5	GND
6	KT SW TA	7	OSC 2	6	GND
7	RESONANCE LATER.	8		7	OUT VOL GEN
8	GND			8	INPUT HEAD PH
				9	GND
				10	OUT HEAD PH

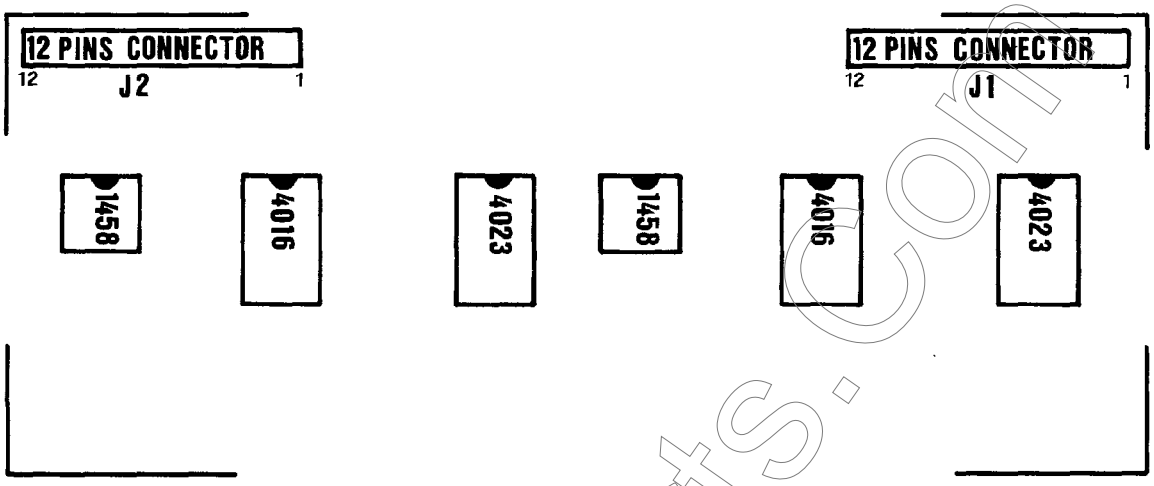
MODEL DS1 DS2 SCHEMA H-I			REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE			



MODEL: DS1–DS2 SCHEMA L			REVISION			
DATE	DRAWN BY Ippolito	DESIGNED BY R Kran	DATE			

DWG6

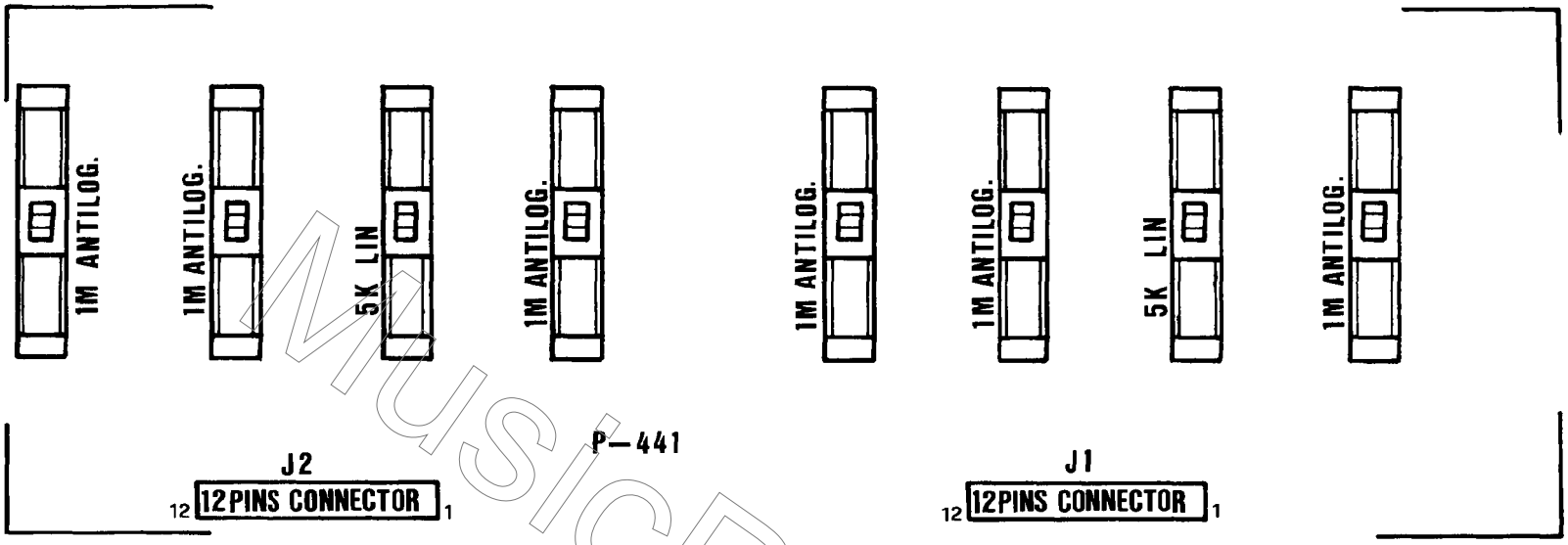
P 440



PIN	REFERENCE J1	PIN	REFERENCE J2
1	+12V	1	OUT ADSR VCF
2	−12V	2	
3	R POT	3	
4	S POT	4	+5V
5	GND	5	R POT
6	GND	6	S POT
7	GND	7	GND
8	GND	8	GND
9	D POT	9	GND
10	A POT	10	GND
11	GATE	11	D POT
12	OUT ADSR VCA	12	A POT

MODEL DS DS SCHEMA L			REVISION	-		
DATE	DRAWN BY Ippolito	DESIGNED BY R Bran	DATE			

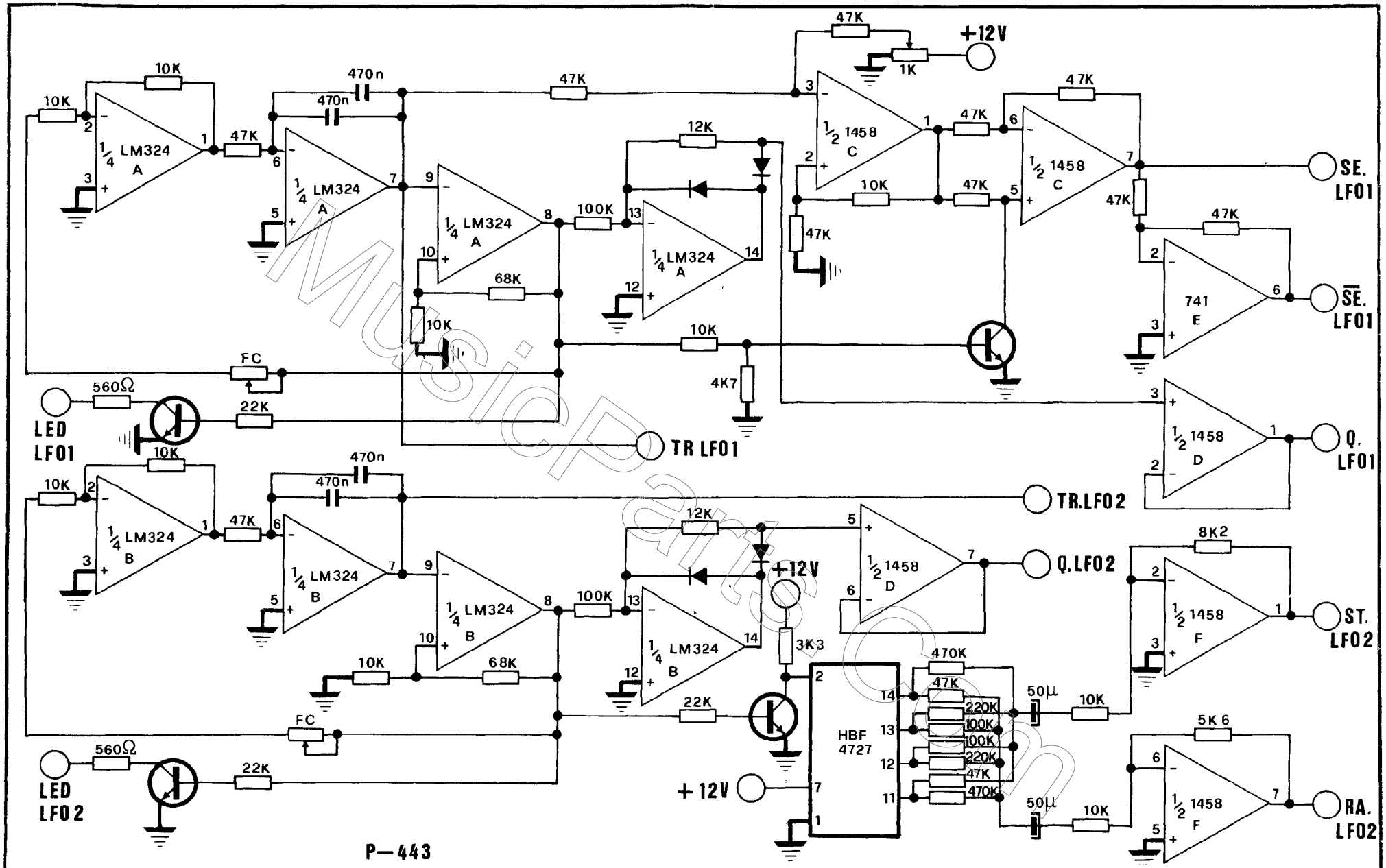
DWG 7



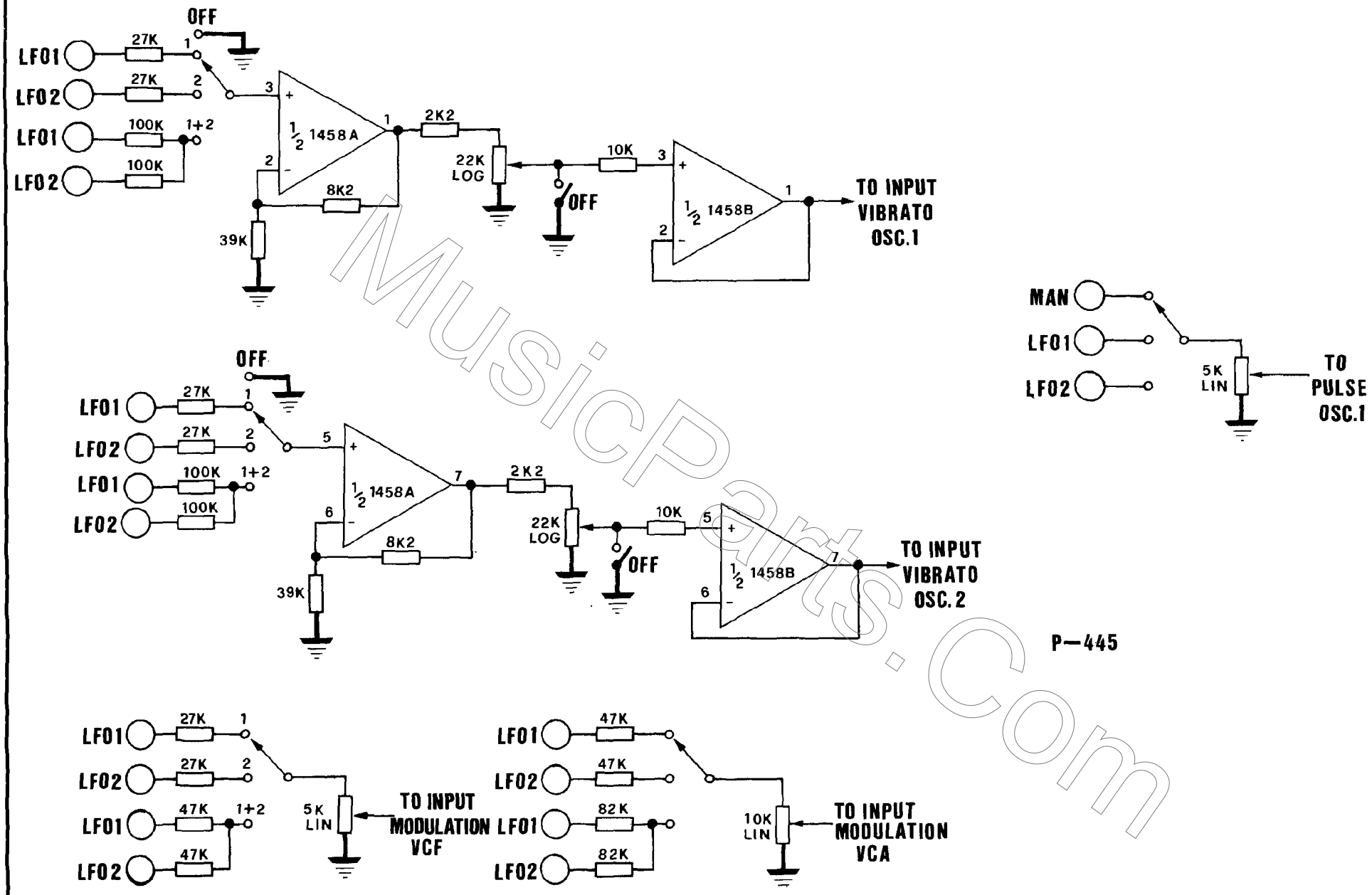
PIN	REFERENCE J2	PIN	REFERENCE J1
1	OUT ADSR VCF	1	+12V
2	" " "	2	-12V
3	" " "	3	R POT.
4	+5V	4	S POT.
5	R POT.	5	GND
6	S POT.	6	"
7	GND	7	"
8	"	8	"
9	"	9	D POT.
10	"	10	A POT.
11	D POT.	11	GATE
12	A POT.	12	OUT ADSR VCA

MODEL	DS2 SCHEMA L		REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE			
	Bordoni G.	R Brani				

DWG 8



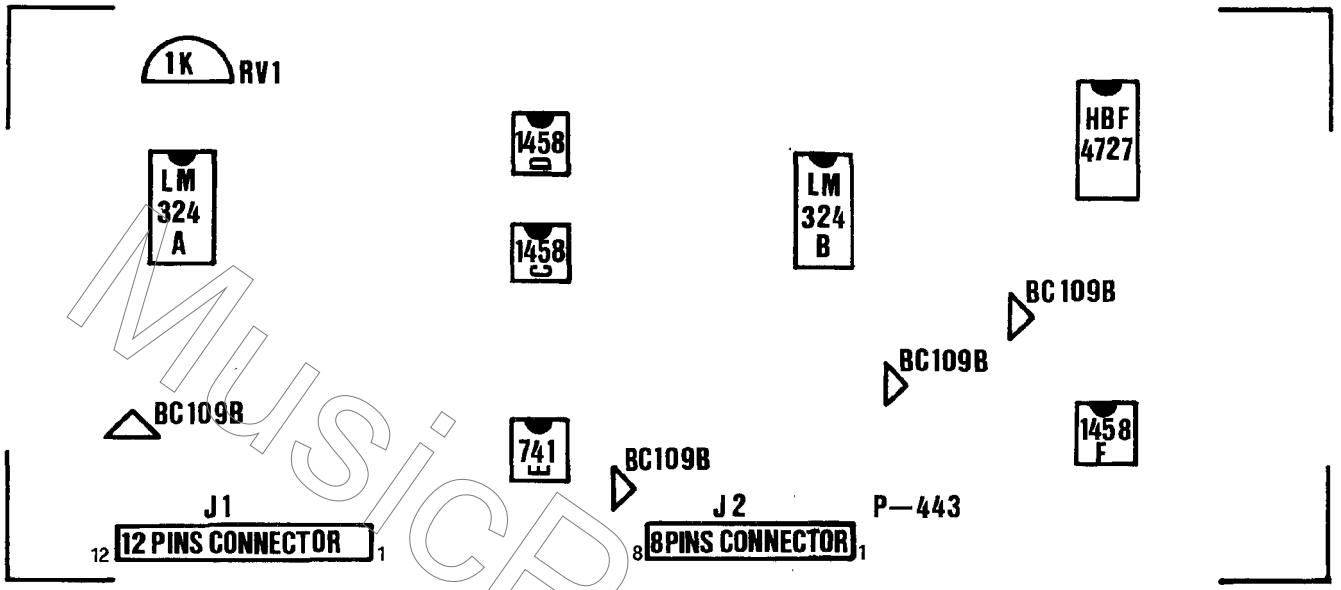
MODEL	DS2 SCHEMA N		REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE			
	Bordini6	R.Bruni				



P—445

MODEL	DS2 SCHEMA M		REVISION			
DATE	DRAWN BY Bordaz G.	DESIGNED BY R Bravi	DATE			

DWG10



PIN	REFERENCE J1
1	$\overline{\text{SE}}$. LFO1
2	SE. LFO1
3	QUADRA LFO1
4	FC LFO1
5	−12V
6	TRI. LFO1
7	GND
8	"
9	"
10	LED LFO1
11	FC LFO1
12	+12V

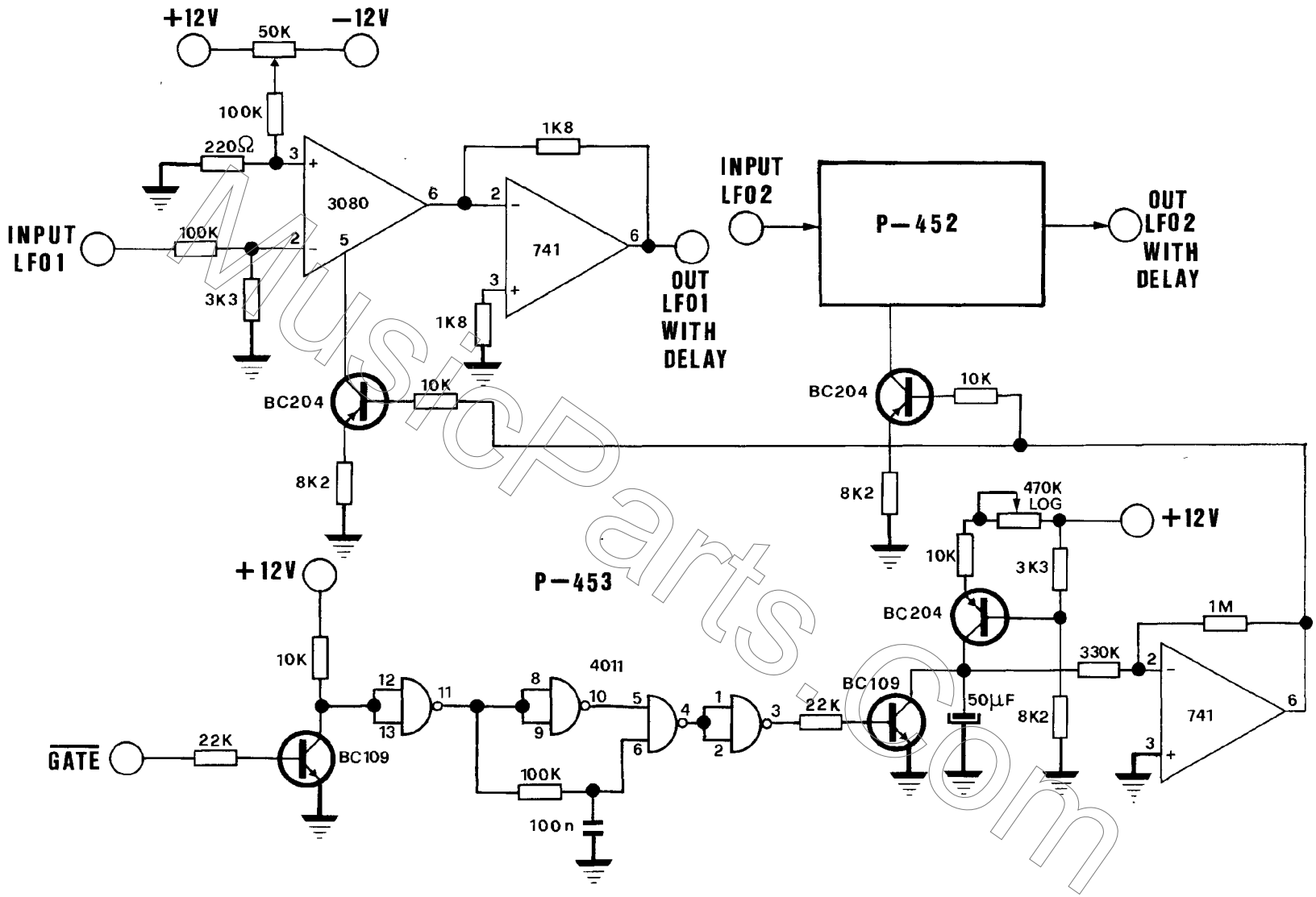
PIN	REFERENCE J2
1	STAIRCASE
2	"
3	SeH
4	LED LFO2
5	FC LFO2
6	QUADRA LFO2
7	TRI. LFO2
8	FC LFO2

MODEL	DS2 SCHEMA N		REVISION			
DATE	DRAWN BY Bordai G.	DESIGNED BY R Borai	DATE			

DWG11

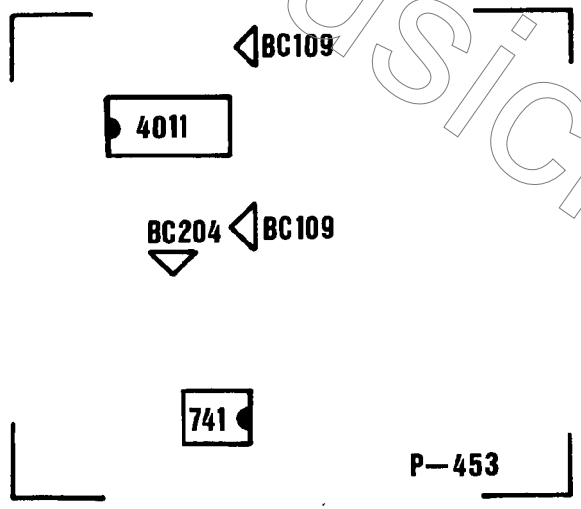
P—445

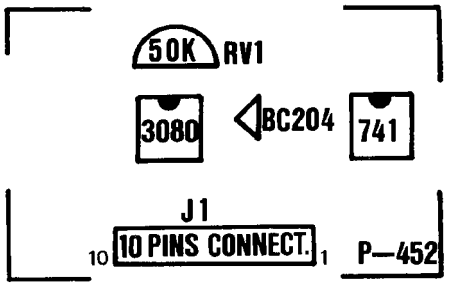
MODEL	DS2 SCHEMA M		REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE			
	Bordoni G.	R Bruni				



MODEL	DS2 SCHEMA Q		REVISION			
DATE	DRAWN BY Bondai G.	DESIGNED BY R Bonai	DATE			

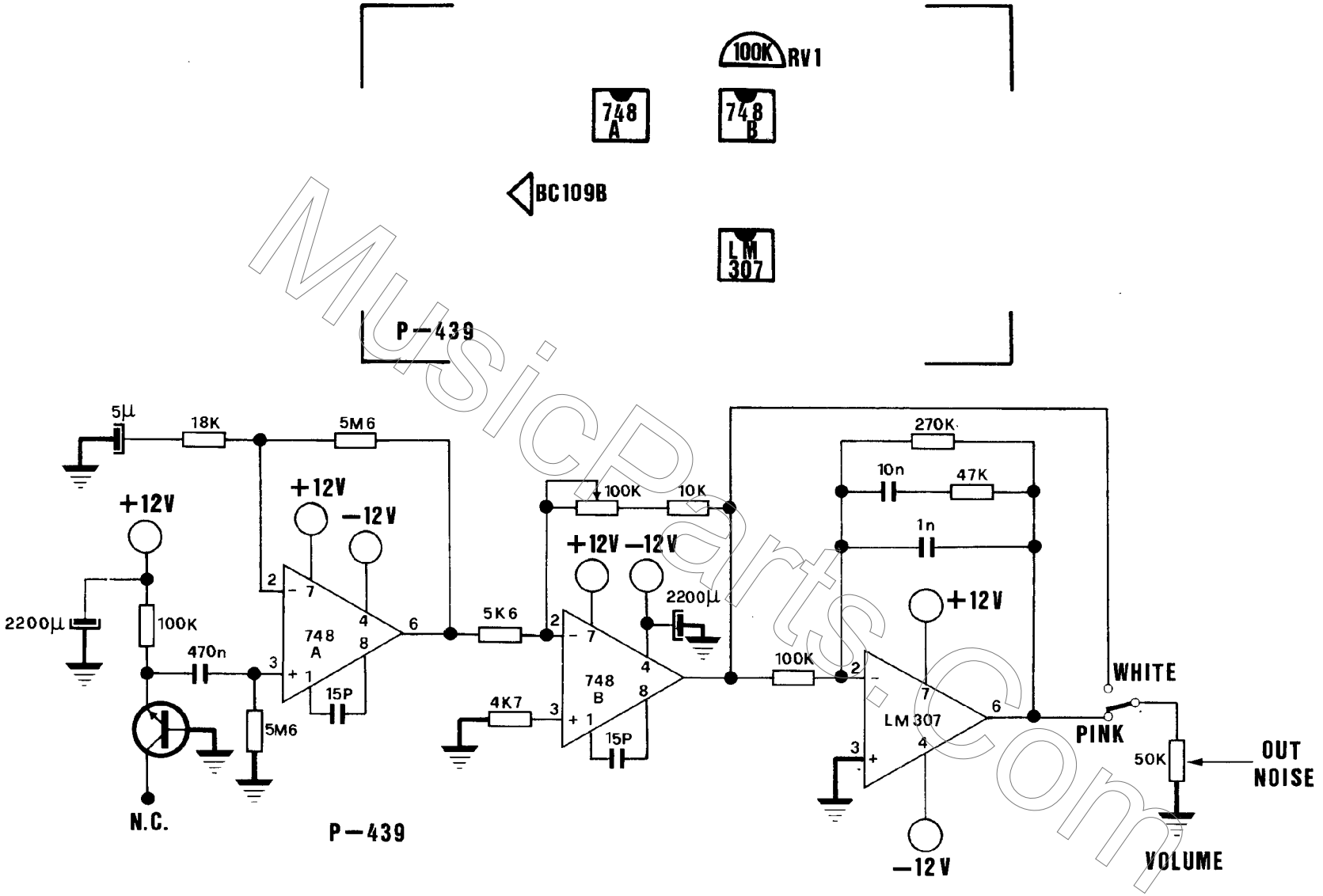
DWG 13





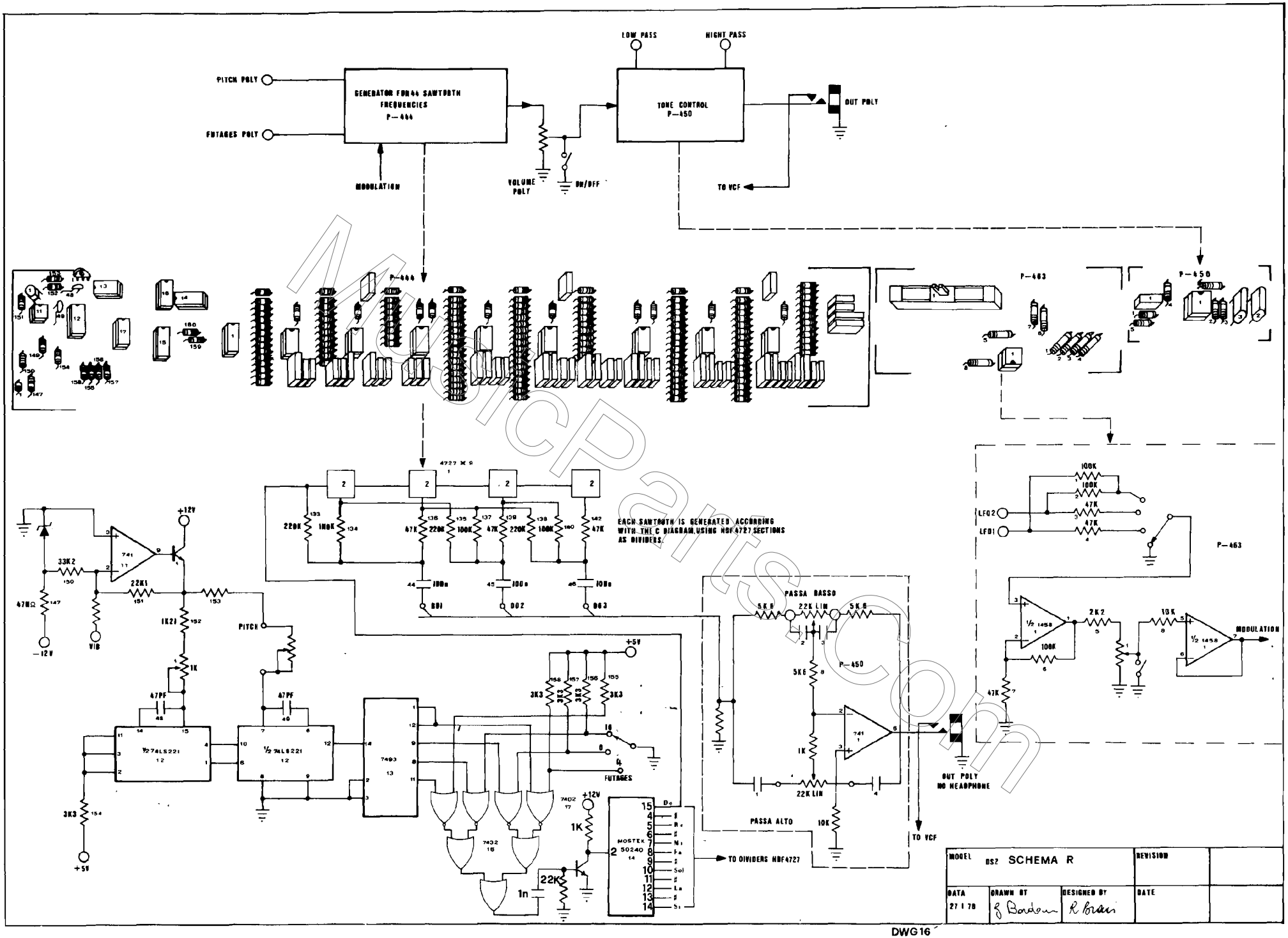
PIN	REFERENCE J1
1	+12V
2	OUT LFO1 or LFO2 WITH DELAY
3	PIN 6 741
4	−12V
5	GND
6	"
7	"
8	INP. LFO1 or LFO2
9	" " " "
10	" " " "

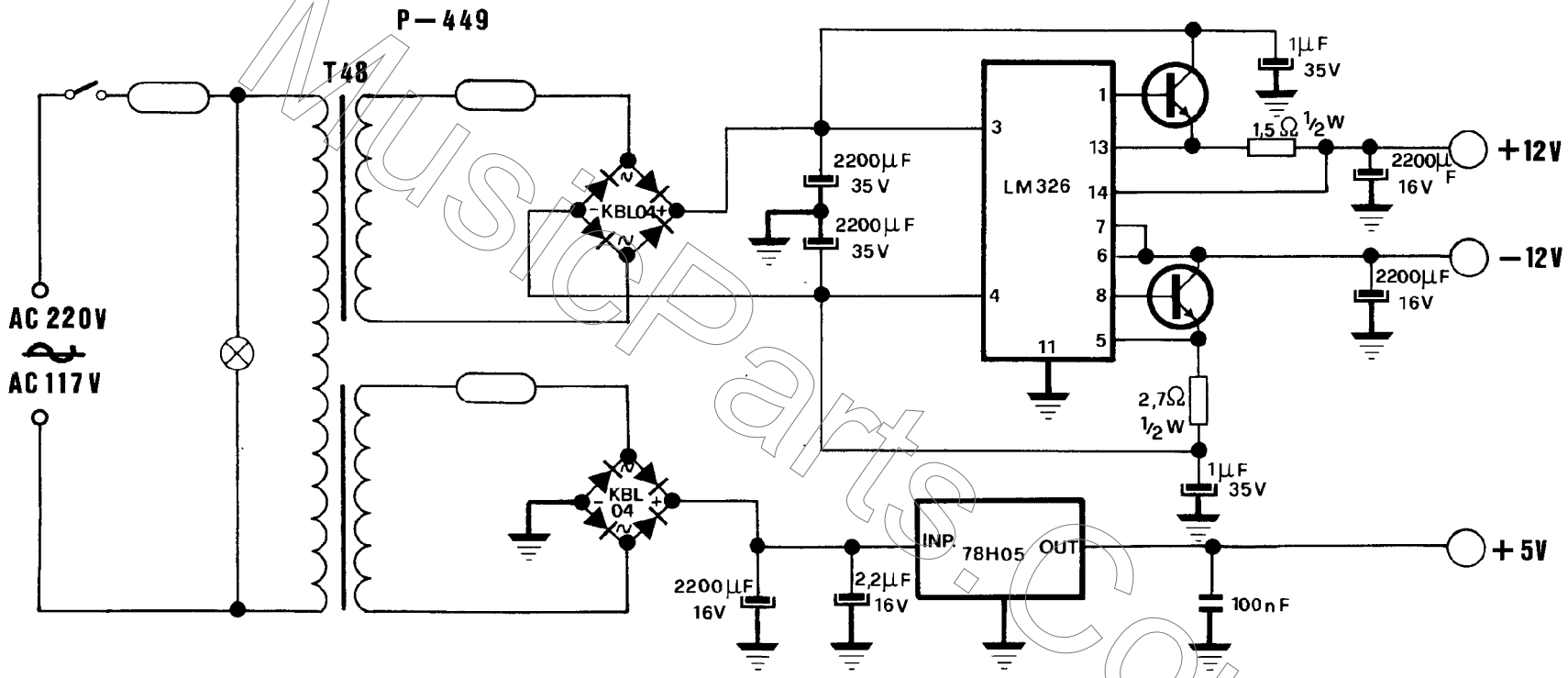
MODEL	DS2 SCHEMA Q		REVISION			
DATE	DRAWN BY Bordai G.	DESIGNED BY R Brari	DATE			



MODEL DS1 DS2 SCHEMA O			REVISION			
DATE	DRAWN BY Bordeni G.	DESIGNED BY R Brain	DATE			

DWG 15


LOW PASS
HIGHT PASS
PITCH POLY
FUTAGES POLY
GENERATOR FOR 44 SAWTOOTH FREQUENCIES P—444
MODULATION
VOLUME POLY
ON/OFF
TONE CONTROL P—450
OUT POLY
TO VCF
P—444
P—463
P—450
4727 X 9
EACH SAWTOOTH IS GENERATED ACCORDING WITH THE C DIAGRAM,USING HDF4727 SECTIONS AS DIVIDERS.
PASSA BASSO
PASSA ALTO
P—450
OUT POLY NO HEADPHONE
TO VCF
LFO2
LFO1
P—463
MODULATION
PITCH
FUTAGES
TO DIVIDERS HDF4727
MOSTEK 50240
MODEL BS2 SCHEMA R
REVISION
DATA 27 1 78
DRAWN BY
DESIGNED BY
DATE
DWG16

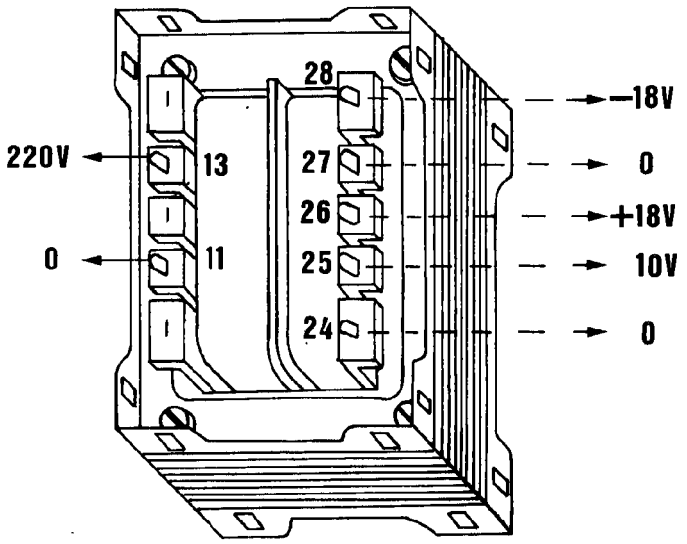


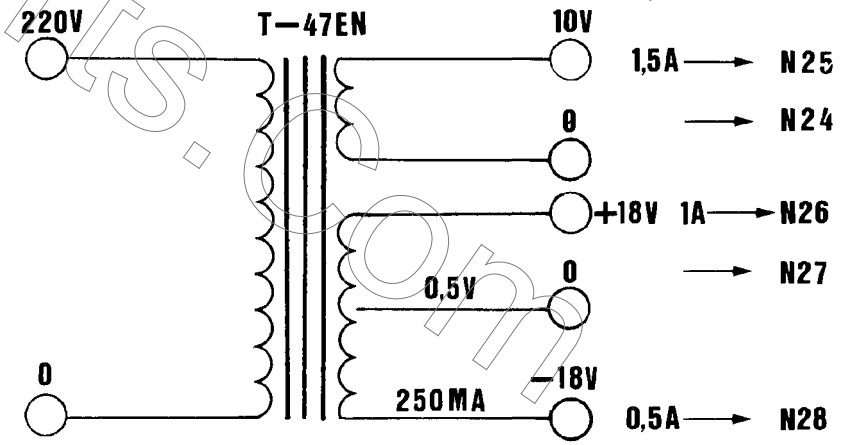
MODEL	DS 2 SCHEMA P		REVISION			
DATE	DRAWN BY Bordai G.	DESIGNED BY R Bordai	DATE			

DWG17

LM
326

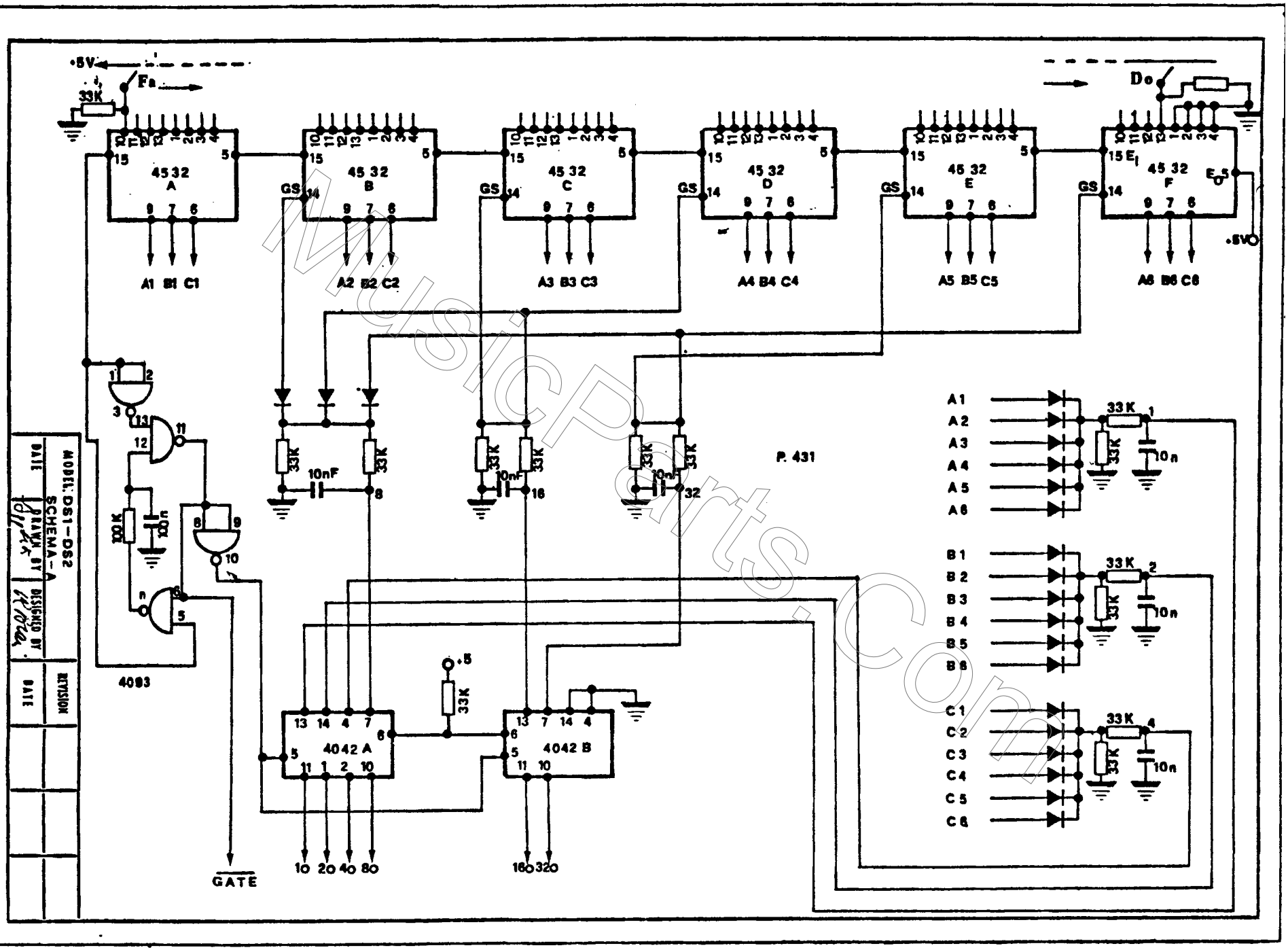
P—449



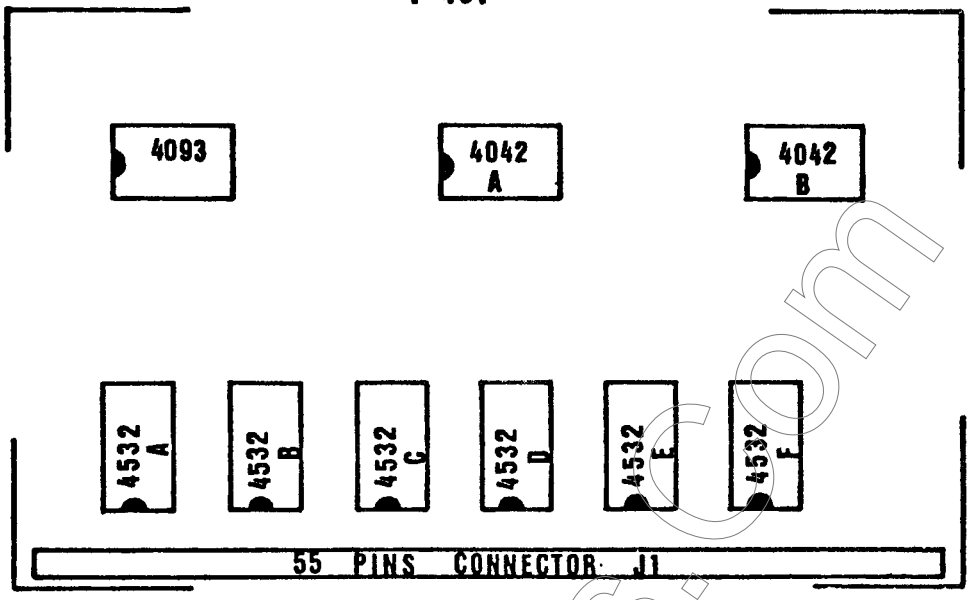


MODEL	DS 2 SCHEMA P		REVISION			
DATE	DRAWN BY Bordoni G.	DESIGNED BY R Brain	DATE			

DWG 18

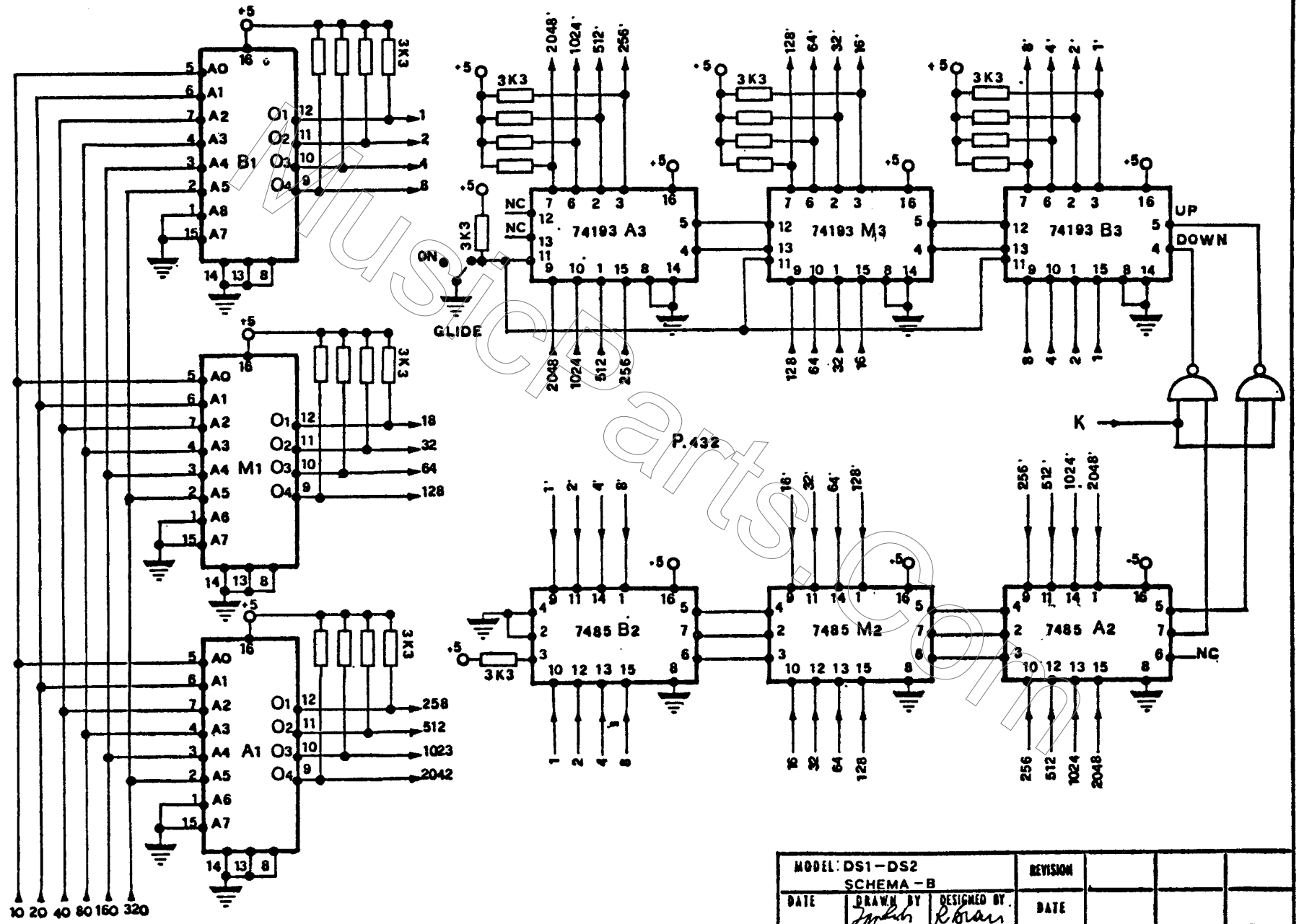


P 431



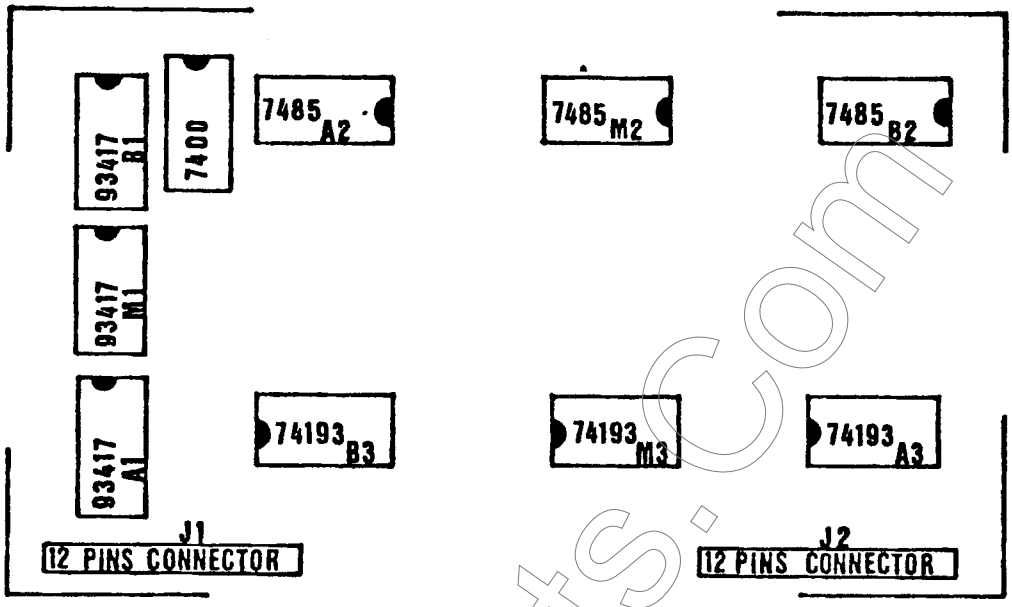
PIN	REFERENCE J1	PIN	REFERENCE J1
1	Fa	28	Sol#
2	Fa#	29	La
3	Sol	30	La#
4	Sol#	31	Si
5	La	32	Do
6	La#	33	Do#
7	Si	34	Re
8	Do	35	Re#
9	Do#	36	Mi
10	Re	37	Fa
11	Re#	38	Fa#
12	Mi	39	Sol
13	Fa	40	Sol#
14	Fa#	41	La
15	Sol	42	La#
16	Sol#	43	Si
17	La	44	Do
18	La#	45	+5V
19	Si	46	GND
20	Do	47	1o
21	Do#	48	2o
22	Re	49	4o
23	Re#	50	8o
24	Mi	51	16o
25	Fa	52	32o
26	Fa#	53	+5V
27	Sol	54	GND
		55	GATE NEG

MODEL DS1 DS2 SCHEMA A			REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE			



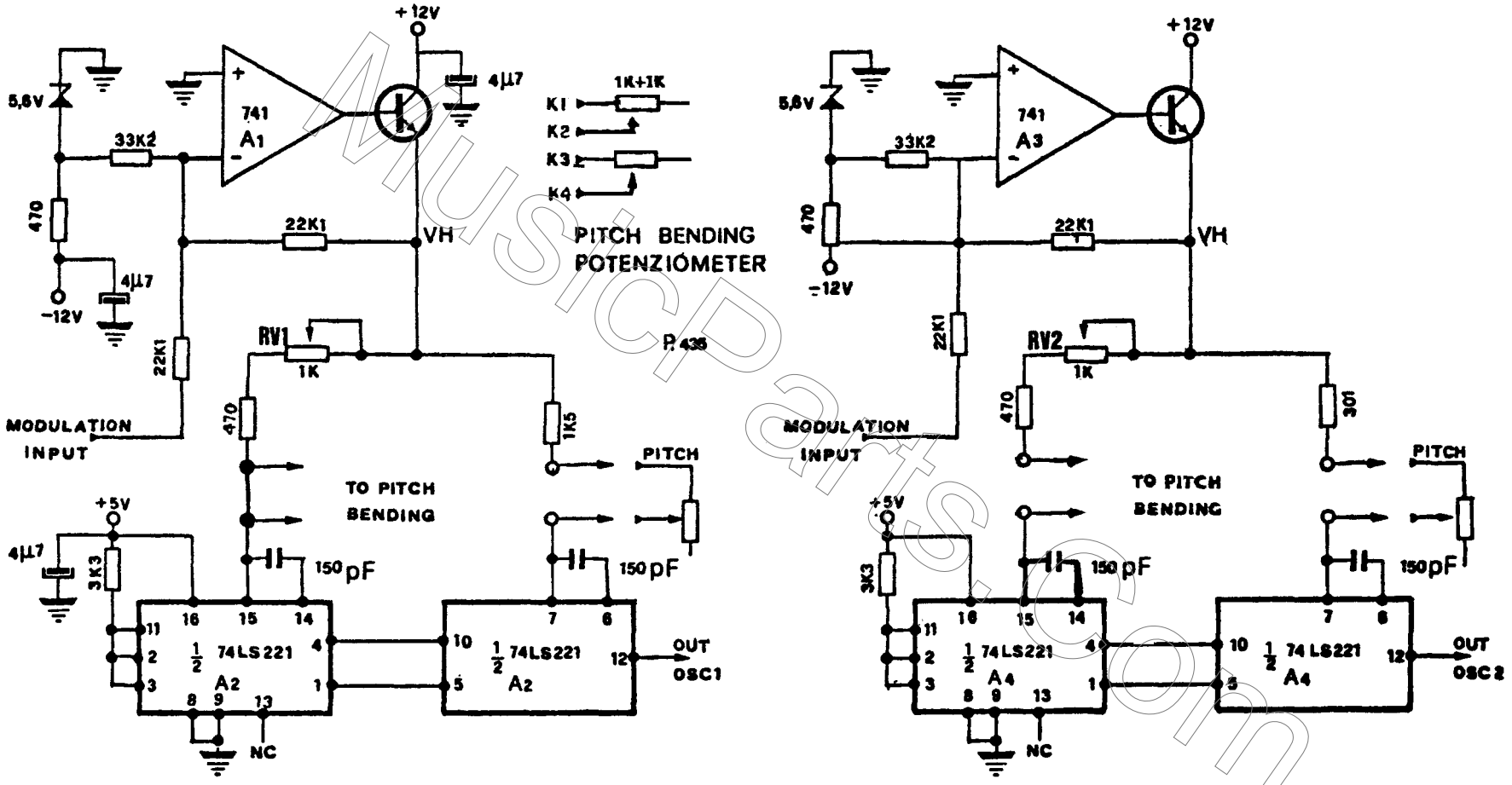
MODEL: DS1–DS2 SCHEMA – B			REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE			

P 432



PIN	REFERENCE J1	PIN	REFERENCE J2
1	1o	1	2048'
2	2o	2	1024'
3	4o	3	512'
4	8o	4	256'
5	16o	5	128'
6	32o	6	64'
7	GND	7	32'
8	GND	8	16'
9	+5V	9	8'
10	K	10	4'
11	PORT SW	11	2'
12		12	1'

MODEL DS1 DS2 SCHEMA B			REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE			

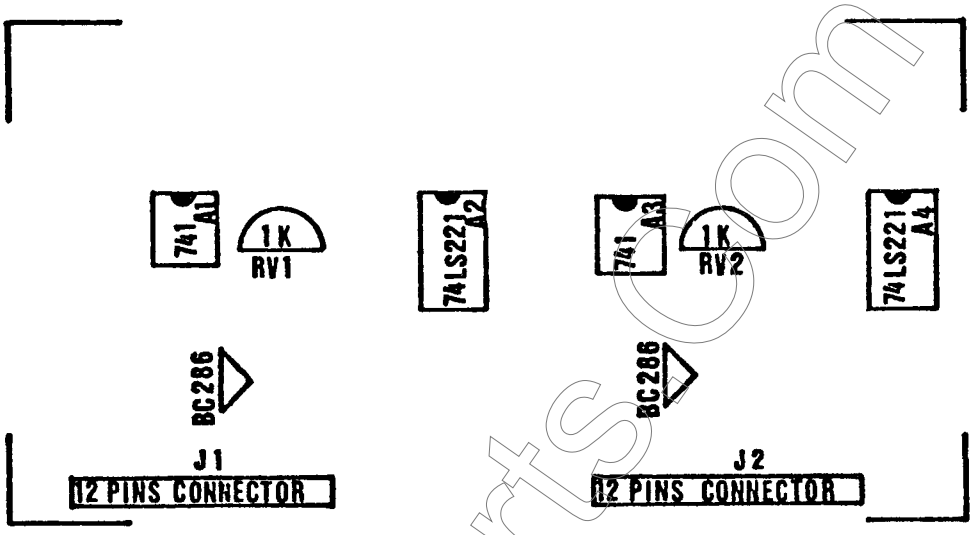


OSCILLATOR 1

OSCILLATOR 2

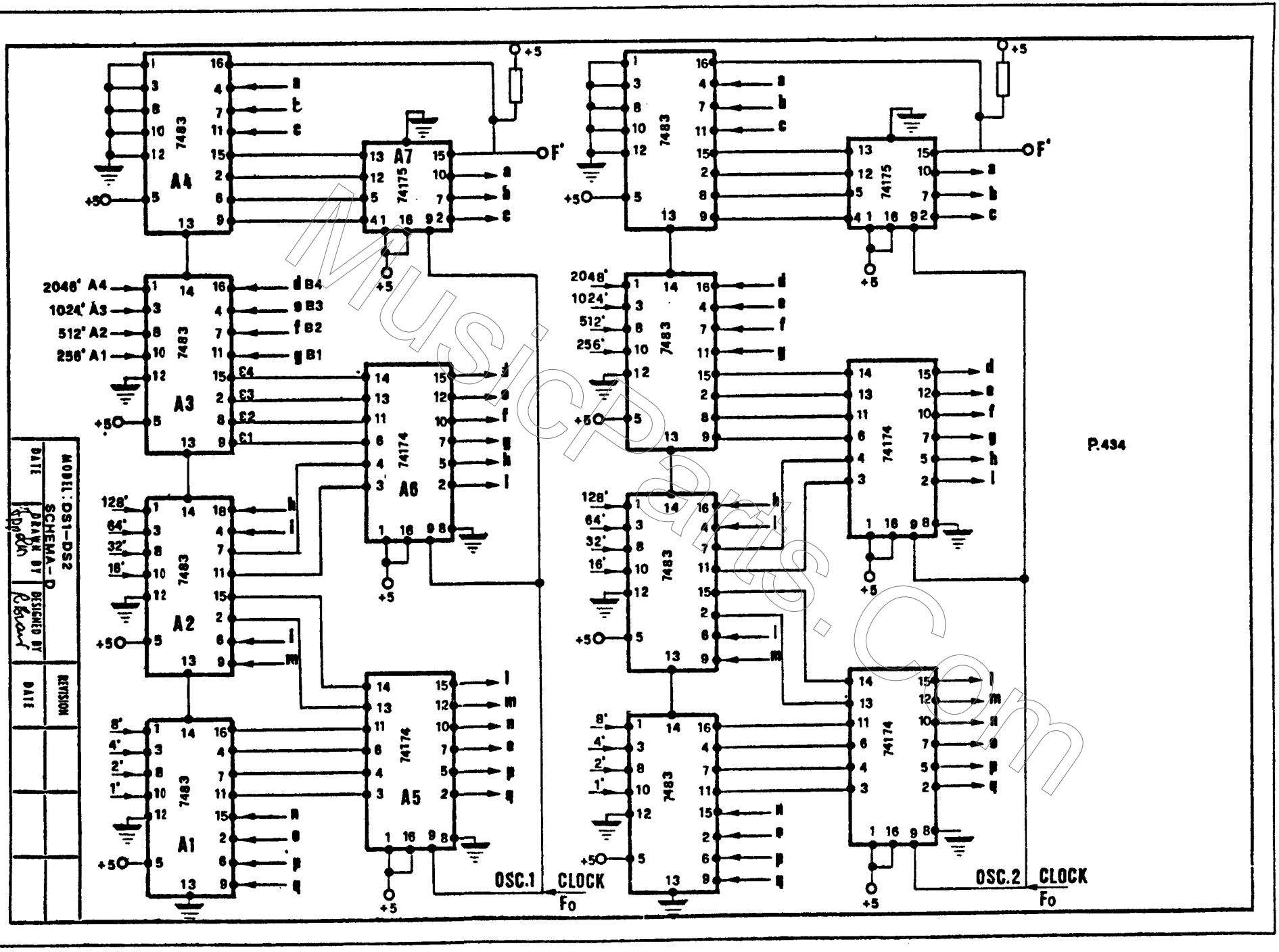
MODEL: DS1-DS2 SCHEMA-C			REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE			

P 435

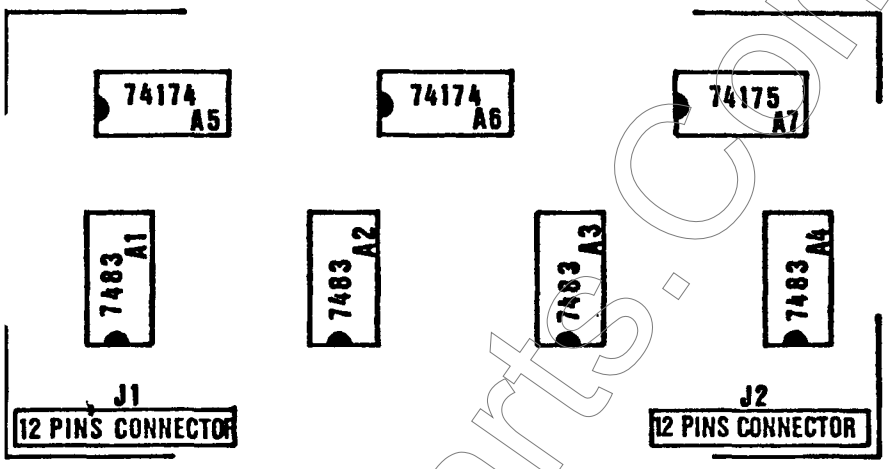


PIN	REFERENCE J1	PIN	REFERENCE J2
1	GND	1	GND
2	GND	2	GND
3	GND	3	GND
4	−12V	4	−12V
5	MOD INPUT	5	MOD INPUT
6	+12V	6	+12V
7	K1	7	K3
8	K2	8	K4
9	+5V	9	+5V
10	OSC1 OUT	10	OSC2 OUT
11	PITCH	11	PITCH
12	PITCH	12	PITCH

MODEL DS DS SCHEMA C			REVISION			
DATE	DRAWN BY	DESIGNED BY,	DATE			

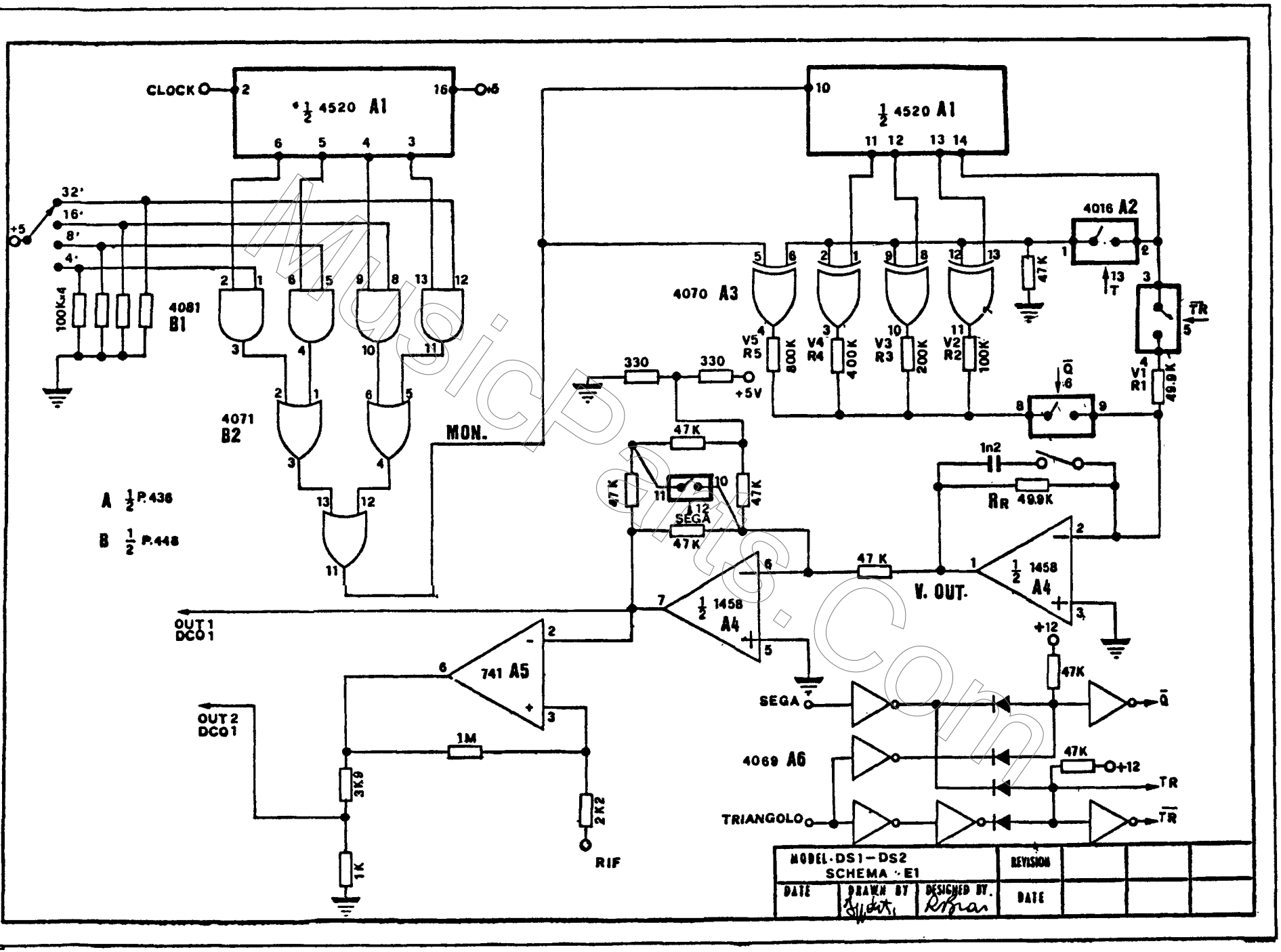

A4
A7
A3
A6
A2
A5
A1
7483
74175
74174
+5
F'
2048' A4
1024' A3
512' A2
256' A1
B4
B3
B2
B1
128'
64'
32'
16'
8'
4'
2'
1'
OSC.1
CLOCK
Fo
OSC.2
CLOCK
Fo
P.434
MODEL: OSI-DS2
SCHEMA-D
DESIGNED BY
DRAWN BY
DATE
REVISION

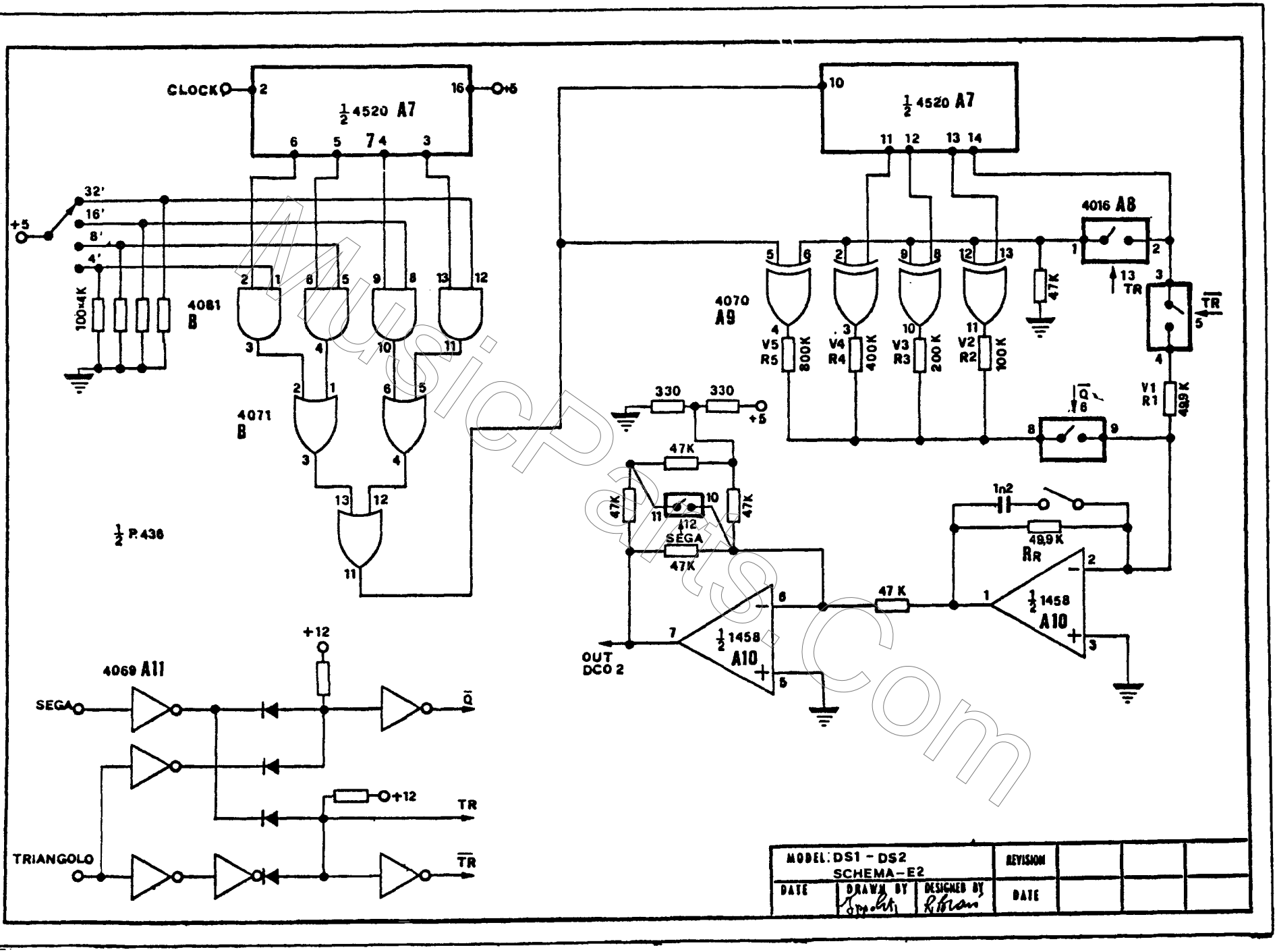
P 434



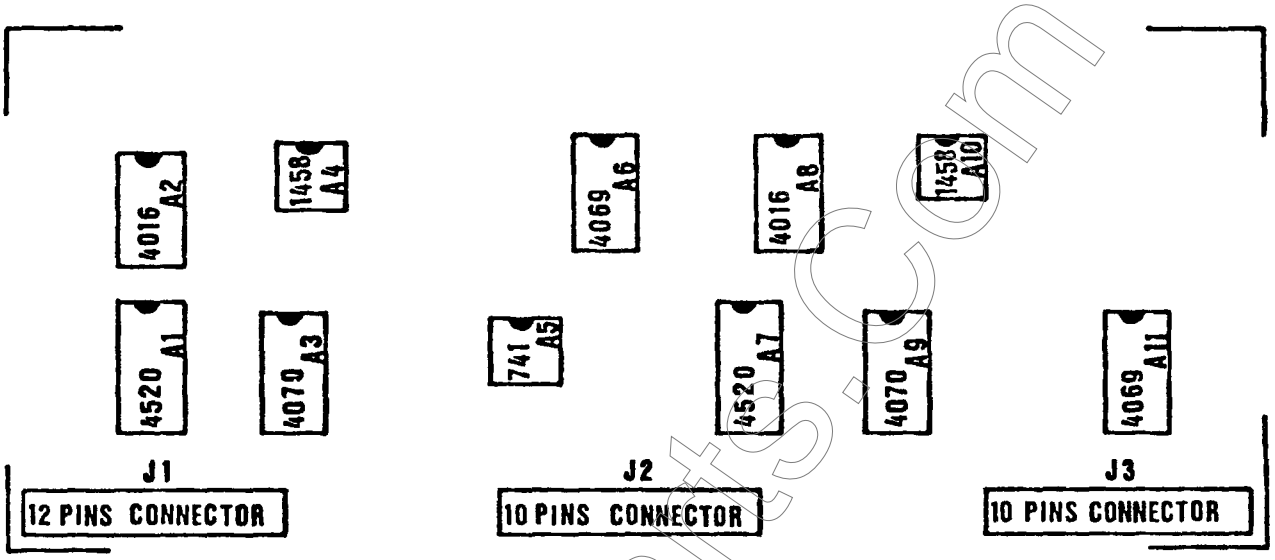
PIN	REFERENCE J1	PIN	REFERENCE J2
1	1'	1	+5V
2	2'	2	+5V
3	4'	3	GND
4	8'	4	GND
5	16'	5	CLOK F_0
6	32'	6	CLOK F_0
7	64'	7	GND
8	128'	8	GND
9	256'	9	OUT F'
10	512'	10	OUT F'
11	1024'	11	NC
12	2048'	12	NC

MODEL DS1 DS2 SCHEMA D			REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE			


CLOCK
½ 4520 A1
½ 4520 A1
4016 A2
4070 A3
4081 B1
4071 B2
MON.
SEGA
V. OUT.
½ 1458 A4
½ 1458 A4
741 A5
4069 A6
TRIANGOLO
RIF
OUT 1 DCO 1
OUT 2 DCO 1
A ½ P.436
B ½ P.448
MODEL · DS1 – DS2
SCHEMA · E1
REVISION
DATE
DRAWN BY
DESIGNED BY


CLOCK
½ 4520 A7
32'
16'
8'
4'
+5
100÷4K
4081 B
4071 B
½ P.436
4069 A11
SEGA
TRIANGOLO
+12
TR
4070 A9
4016 A8
13 TR
330
47K
SEGA
1n2
49,9K
RR
47 K
½ 1458 A10
OUT DCO 2
V5 R5 800K
V4 R4 400K
V3 R3 200 K
V2 R2 100 K
V1 R1 49,9 K
MODEL: DS1 - DS2
SCHEMA - E2
REVISION
DATE
DRAWN BY
DESIGNED BY

P 436

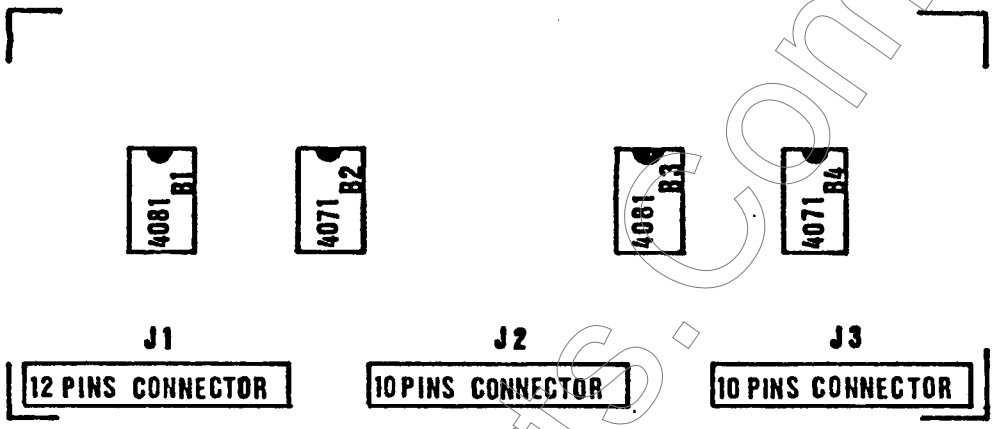


PIN	REFERENCE J1	PIN	REFERENCE J2	PIN	REFERENCE J3
1	COND	1	V. RIF	1	MON OSC2
2	COND	2	OUT1 DCO1	2	SEGA
3	F' OSC1	3	OUT2 DCO1	3	GND
4	4' FUTAGES	4	SEGA WAVEF SW	4	GND
5	8' SW	5	TRIAN OSC 1	5	GND
6	16' OSC 1	6	F' OSC1	6	GND
7	32'	7	4' FUTAGES	7	GND
8	GND	8	8' SW	8	GND
9	MON OSC1	9	16' OSC 1	9	TRIANG
10	+5V	10	32'	10	OUT DCO2
11	+12V				
12	−12V				

WAVEF SW OSC 1

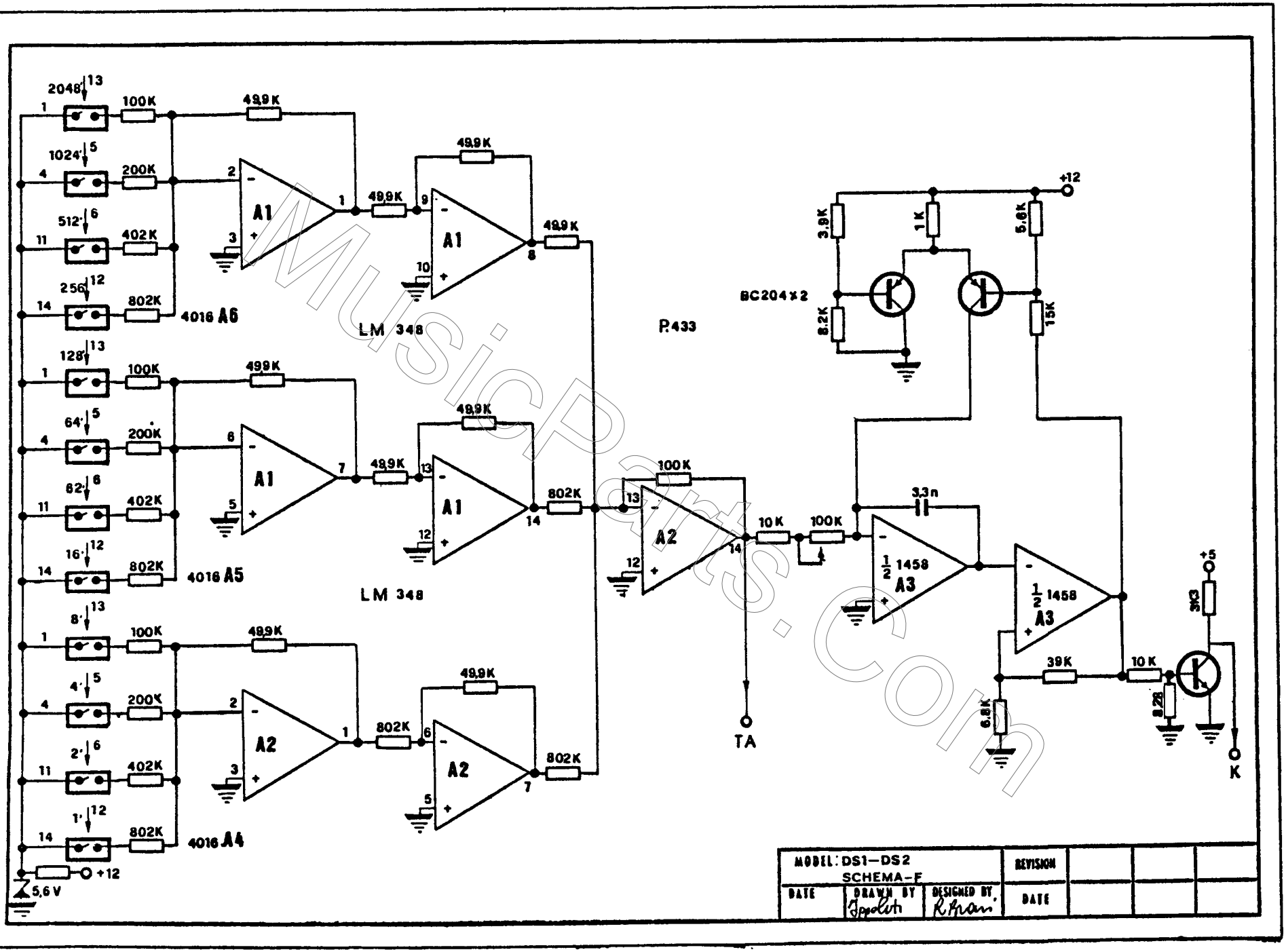
MODEL DS1 DS2 SCHEMA E			REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE			

P 448

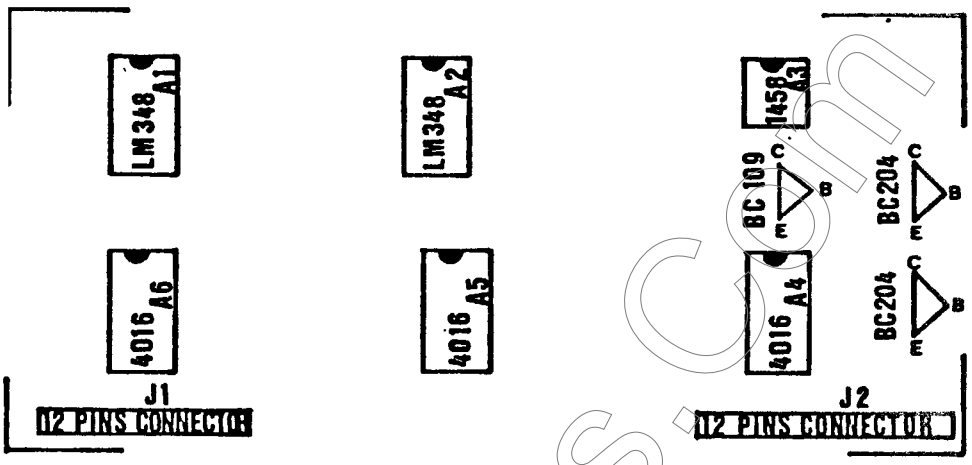


PIN	REFERENCE J1	PIN	REFERENCE J2	PIN	REFERENCE J3
1	COND	1	V. RIF	1	MON OSC2
2	COND	2	OUT1 DCO1	2	SEGA → WAVEF SW
3	F' OSC1	3	OUT2 DCO1	3	GND
4	4' FUTAGES	4	SEGA WAVEF SW	4	GND
5	8' SW	5	TRIANG F' OSC1	5	GND
6	16' OSC 1	6	F' OSC1	6	GND
7	32'	7	4' FUTAGES	7	GND
8	GND	8	8' SW	8	GND
9	MON OSC 1	9	16' OSC1	9	TRIANG → OSC 1
10	+5	10	32'	10	OUT DCO2
11	+12				
12	−12				

MODEL DS1 DS2 SCHEMA E			REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE			


2048
1024
512
256
128
64
32
16
8
4
2
1
100K
200K
402K
802K
49.9K
4016 A6
4016 A5
4016 A4
LM 348
LM 348
A1
A2
P.433
BC204x2
3.9K
1K
5.6K
8.2K
15K
+12
100K
10K
3.3n
A2
A3
1/2 1458
39K
6.8K
3K3
8.2K
+5
TA
K
5,6 V
MODEL: DS1–DS2
SCHEMA-F
REVISION
DATE
DRAWN BY
DESIGNED BY

P 433



PIN	REFERENCE J1	PIN	REFERENCE J2
1	+12V	1	2048'
2	GND	2	1024'
3	GND	3	512'
4	+5	4	256'
5	+5	5	128'
6	K	6	64'
7	K	7	32'
8	TA	8	16'
9	TA	9	8'
10	-12V	10	4'
11	GLIDE RATE	11	2'
12	GLIDE RATE	12	1'

MODEL DS1 DS2 SCHEMA F			REVISION			
DATE	DRAWN BY Byrch	DESIGNED BY R Brai	DATE			

TAVOLA DELLA VERITA' N.1

	32o	16o	8o	4o	2o	1o
FA	0	0	0	0	0	0
FA"	0	0	0	0	0	1
SOL	0	0	0	0	1	0
SOL"	0	0	0	0	1	1
LA	0	0	0	1	0	0
LA"	0	0	0	1	0	1
SI	0	0	0	1	1	0
DO	0	0	0	1	1	1
DO"	0	0	1	0	0	0
RE	0	0	1	0	0	1
RE"	0	0	1	0	1	0
MI	0	0	1	0	1	1
FA	0	0	1	1	0	0
FA"	0	0	1	1	0	1
SOL	0	0	1	1	1	0
SOL"	0	0	1	1	1	1
LA	0	1	0	0	0	0
LA"	0	1	0	0	0	1
SI	0	1	0	0	1	0
DO	0	1	0	0	1	1
DO"	0	1	0	1	0	0
RE	0	1	0	1	0	1
RE"	0	1	0	1	1	0
MI	0	1	0	1	1	1
FA	0	1	1	0	0	0
FA"	0	1	1	0	0	1
SOL	0	1	1	0	1	0
SOL"	0	1	1	0	1	1
LA	0	1	1	1	0	0
LA"	0	1	1	1	0	1
SI	0	1	1	1	1	0
DO	0	1	1	1	1	1
DO"	1	0	0	0	0	0
RE	1	0	0	0	0	1
RE"	1	0	0	0	1	0
MI	1	0	0	0	1	1
FA	1	0	0	1	0	0
FA"	1	0	0	1	0	1
SOL	1	0	0	1	1	0
SOL"	1	0	0	1	1	1
LA	1	0	1	0	0	0
LA"	1	0	1	0	0	1
SI	1	0	1	0	1	0
DO	1	0	1	0	1	1

TAVOLA DELLA VERITA' N.2

	93417 A				93417 M				93417 B				Fattori di
	O_4 2048	O_3 1024	O_2 512	O_1 256	O_4 128	O_3 64	O_2 32	O_1 16	O_4 8	O_3 4	O_2 2	O_1 1	moltiplicazione
FA	0	0	0	0	1	1	1	0	1	1	1	1	239
FA"	0	0	0	0	1	1	1	1	1	1	0	1	253
SOL	0	0	0	1	0	0	0	0	1	1	0	0	268
SOL"	0	0	0	1	0	0	0	1	1	1	0	0	284
LA	0	0	0	1	0	0	1	0	1	1	0	1	301
LA"	0	0	0	1	0	0	1	1	1	1	1	1	319
SI	0	0	0	1	0	1	0	1	0	0	1	0	338
DO	0	0	0	1	0	1	1	0	0	1	1	0	358
DO"	0	0	0	1	0	1	1	1	1	0	1	1	379
RE	0	0	0	1	1	0	0	1	0	0	1	0	402
RE"	0	0	0	1	1	0	1	0	1	0	1	0	426
MI	0	0	0	1	1	1	0	0	0	0	1	1	451
FA	0	0	0	1	1	1	0	1	1	1	1	0	478
FA'	0	0	0	1	1	1	1	1	1	0	1	0	506
SOL	0	0	1	0	0	0	0	1	1	0	0	0	536
SOL"	0	0	1	0	0	0	1	1	1	0	0	0	568
LA	0	0	1	0	0	1	0	1	1	0	1	0	602
LA"	0	0	1	0	0	1	1	1	1	1	1	0	638
SI	0	0	1	0	1	0	1	0	0	1	0	0	676
DO	0	0	1	0	1	1	0	0	1	1	0	0	716
DO"	0	0	1	0	1	1	1	1	0	1	1	0	758
RE	0	0	1	1	0	0	1	0	0	1	0	0	804
RE"	0	0	1	1	0	1	0	1	0	1	0	0	852
MI	0	0	1	1	1	0	0	0	0	1	1	0	902
FA	0	0	1	1	1	0	1	1	1	1	0	0	956
FA"	0	0	1	1	1	1	1	1	0	1	0	0	1.012
SOL	0	1	0	0	0	0	1	1	0	0	0	0	1.072
SOL"	0	1	0	0	0	1	1	1	0	0	0	0	1.136
LA	0	1	0	0	1	0	1	1	0	1	0	0	1.204
LA"	0	1	0	0	1	1	1	1	1	1	0	0	1.276
SI	0	1	0	1	0	1	0	0	1	0	0	0	1.352
DO	0	1	0	1	1	0	0	1	1	0	0	0	1.432
DO"	0	1	0	1	1	1	1	0	1	1	0	0	1.516
RE	0	1	1	0	0	1	0	0	1	0	0	0	1.608
RE"	0	1	1	0	1	0	1	0	1	0	0	0	1.704
MI	0	1	1	1	0	0	0	0	1	1	0	0	1.804
FA	0	1	1	1	0	1	1	1	1	0	0	0	1.912
FA"	0	1	1	1	1	1	1	0	1	0	0	0	2.024
SOL	1	0	0	0	0	1	1	0	0	0	0	0	2.144
SOL"	1	0	0	0	1	1	1	0	0	0	0	0	2.272
LA	1	0	0	1	0	1	1	0	1	0	0	0	2.408
LA"	1	0	0	1	1	1	1	1	1	0	0	0	2.552
SI	1	0	1	0	1	0	0	1	0	0	0	0	2.704
DO	1	0	1	1	0	0	1	1	0	0	0	0	2.864

TAVOLE DELLA VERITA' N° 4

		T.A.
FA	239	-0.62 V
FA"	253	-0.65 V
SOL	268	-0.70 V
SOL"	284	-0.74 V
LA	301	-0.79 V
LA"	319	-0.83 V
SI	338	-0.89 V
DO	358	-0.94 V
DO"	379	-1 V
RE	402	-1.06 V
RE"	426	-1.13 V
MI	451	-1.19 V
FA	478	-1.27 V
FA"	506	-1.34 V
SOL	536	-1.43 V
SOL"	568	-1.52 V
LA	602	-1.61 V
LA"	638	-1.71 V
SI	676	-1.81 V
DO	716	-1.92 V
DO"	758	-2.03 V
RE	804	-2.16 V
RE"	852	-2.29 V
MI	902	-2.42 V
FA	956	-2.56 V
FA"	1012	-2.73 V
SOL	1072	-2.90 V
SOL"	1136	-3.07 V
LA	1204	-3.26 V
LA"	1276	-3.46 V
SI	1352	-3.66 V
DO	1432	-3.88 V
DO"	1515	-4.11 V
RE	1608	-4.36 V
RE"	1704	-4.62 V
MI	1804	-4.90 V
FA	1912	-5.19 V
FA"	2024	-5.50 V
SOL	2144	-5.85 V
SOL"	2272	-6.20 V
LA	2408	-6.57 V
LA"	2552	-6.96 V
SI	2704	-7.38 V
DO	2854	-7.80 V

Keyboard Control Voltages